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# TMS3615NS

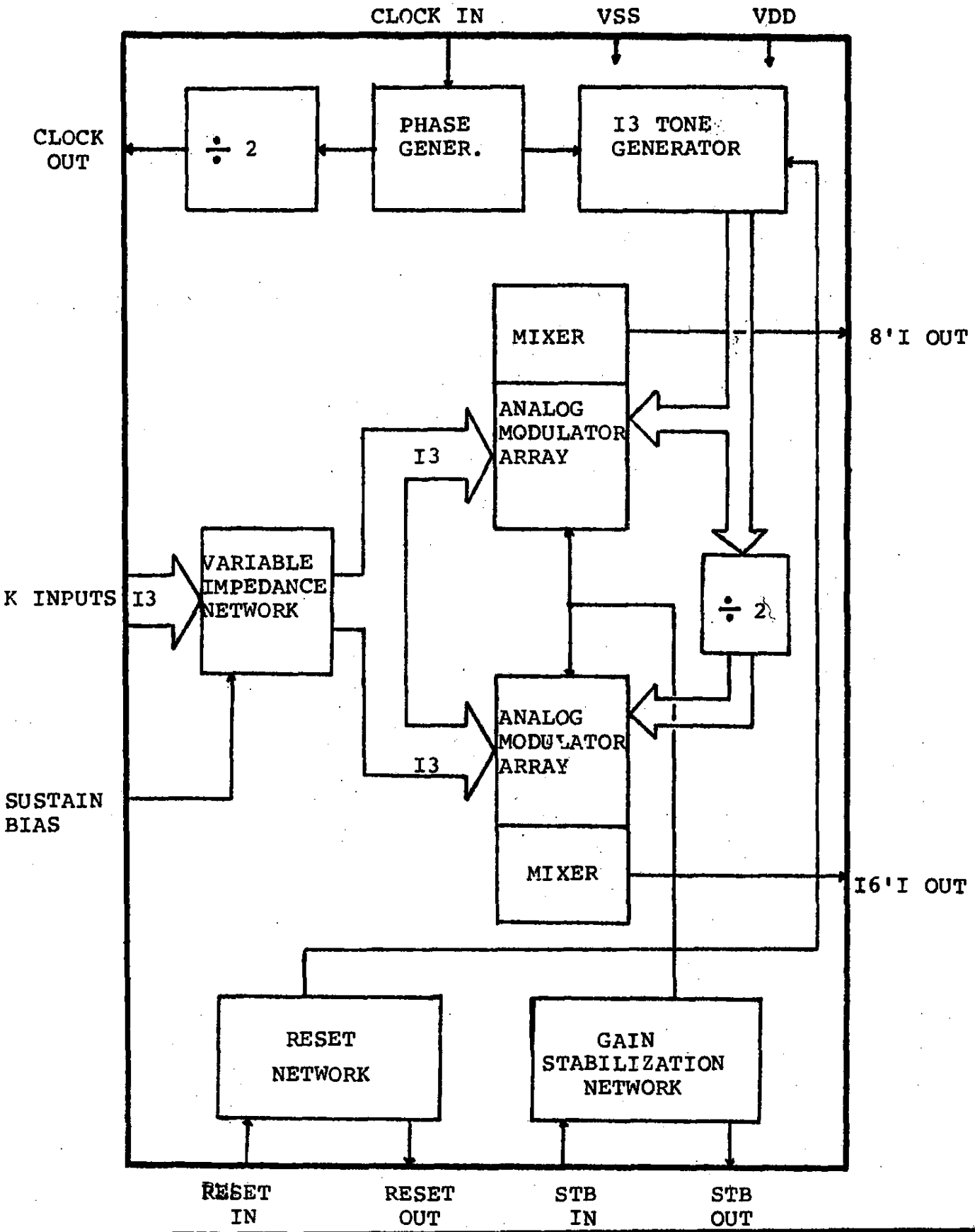
# OCTAVE MULTIPLE TONE SYNTHESIZER - OMTS

(2 FOOTAGES)

NOVEMBER 1981

- 2 footages (16', 8', or 8', 4' or 4', 2') current outputs
- Sustain of the output signals is possible by simply connecting a capacitor (1 /uF) to each key input
- Sustain decay time adjustable from a few ms to a very long time (key memorization) by connecting a variable voltage to the appropriate terminal
- Possibility of controlling the amplitude swing of the footage outputs, to minimize the spread among different devices, by connecting a simple external network to the appropriate terminals
- Asynchronous reset to synchronize devices of different octaves
- Single power supply (15V or 12V typical)
- Clock output for lower octave device

## BLOCK DIAGRAM



## CIRCUIT DESCRIPTION

There is a tone generator, that produces 13 acoustic frequencies for the higher footage (8'), and 13 toggles that divide these frequencies by two for the lower footage (16').

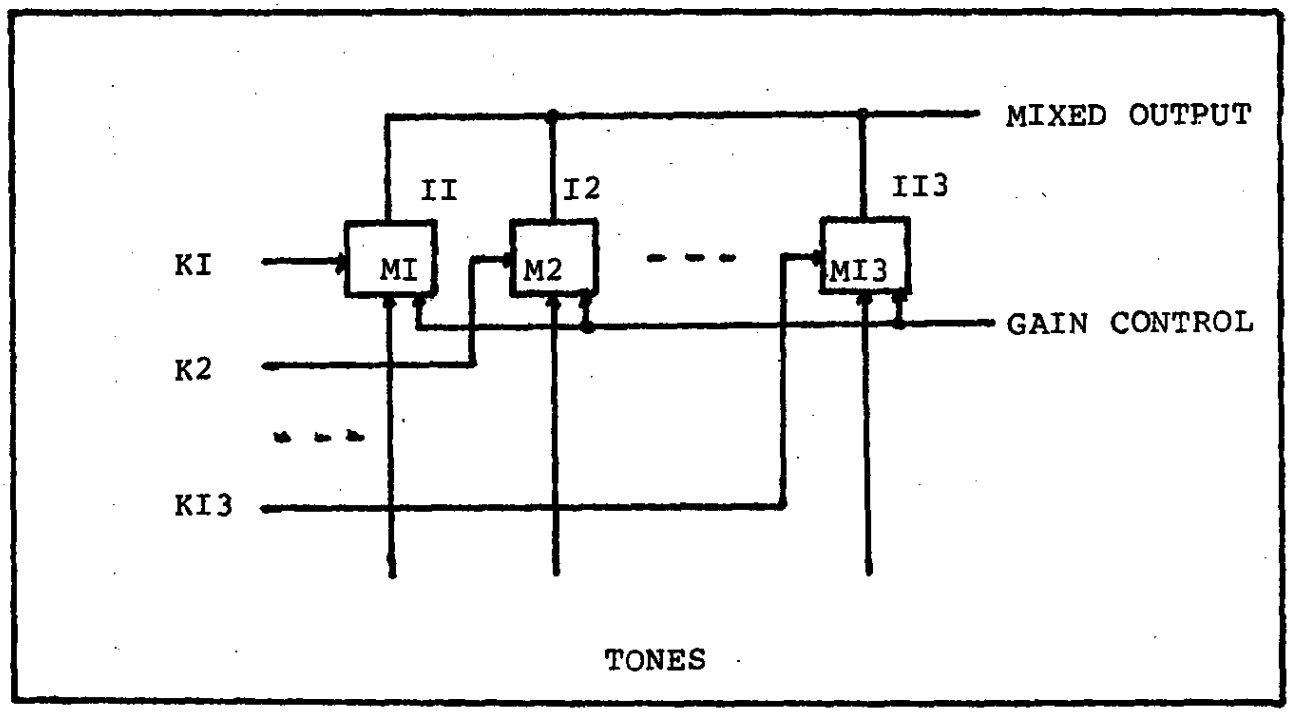
The actual frequency of the tones depends on the input clock.

A clock output (half of the frequency of the clock input) is provided to be used as clock input to the next lower octave devive.

The pull-up impedance of the key inputs is programmable from a low value to an open circuit value by properly biasing the Sustain Bias input.

The k inputs go in parallel to the Analog Modulator Array blocks of the two footages.

Each of these blocks contains 13 identical current output analog modulators as shown in fig.



Each modulator produces an acoustic carrier (Tone), amplitude modulated from 0% to 100% by the corresponding k input voltage, around a constant d.c. level (offset current) equal to one half the maximum swing of each modulator output.

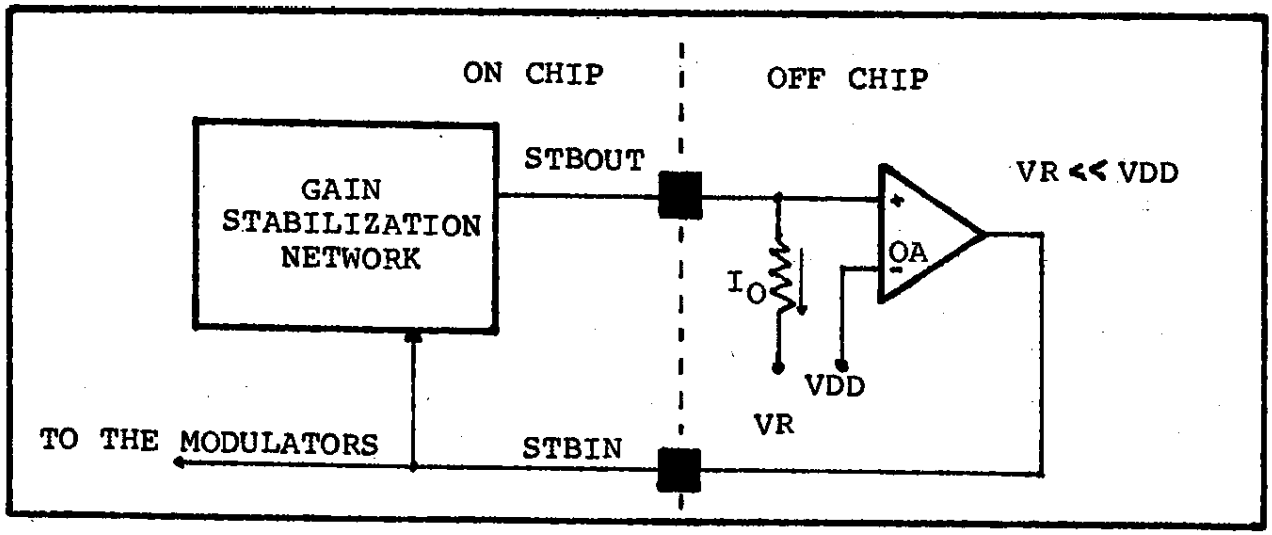
These outputs are then summed together, instant by instant, to provide a single composite output current given by:

$$I_{out} = \sum_{k=1}^{13} (I_o + C\ Vk\ Fk)$$

Where:

- $I_o$ is the modulator output current (200 uA typical) with the k input at Vss.
- C is a constant
- Vk are the voltages on the k inputs, with respect of Vss.
- Fk are functions whose value are +1 or -1 according to the internal tone waveforms ("1", "0" logic).

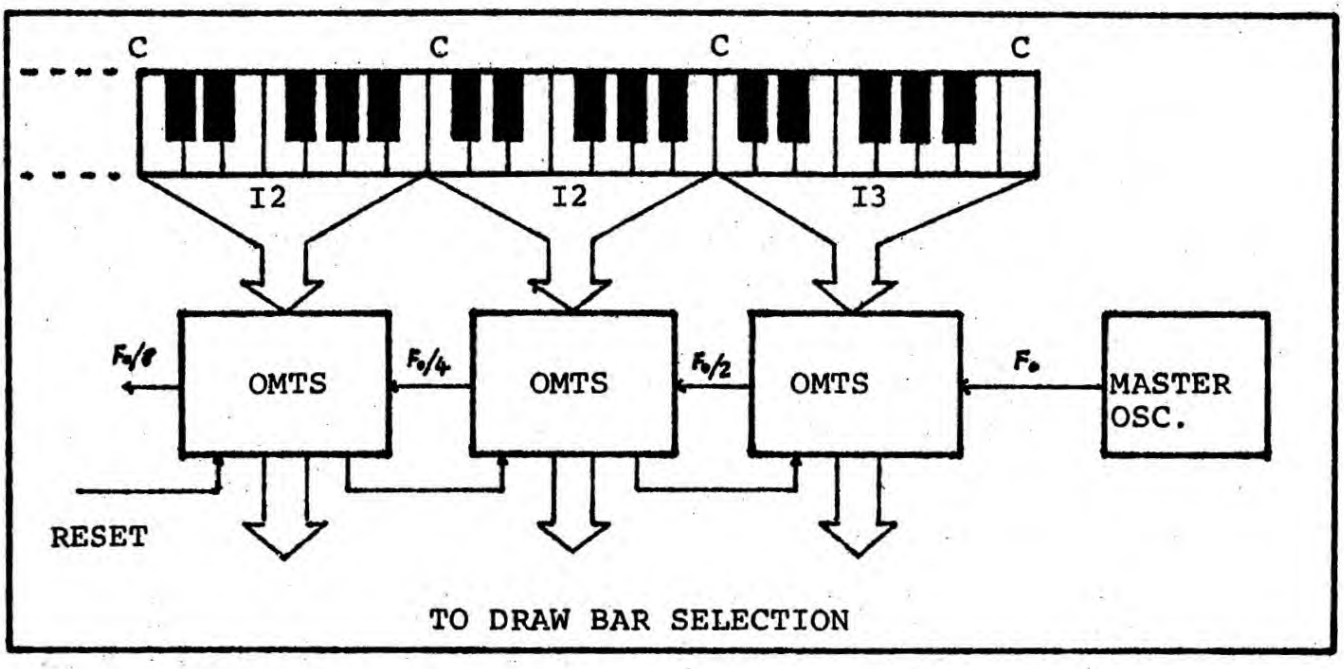
The mean value of each modulator's output is equal to $I_o$ while the signal component C Vk Fk is equal to $\pm I_o$ if Vk is equal to $V_{DD}$. In order to make this $I_o$ value independent from temperature and constant, among different devices serving different octaves, each modulator has a gain control (STBIN) coming from the GAIN STABILIZATION NETWORK. This network provides automatic gain control (A.G.C.). When used in conjunction with an external amplifier that senses the current on the output STBOUT (this current is equal to $I_o$) and automatically adjusts the STBIN voltage to maintain this current constant, as shown in Fig



TMS36I5 NS - RI107-RI103

The TMS36I5NS is a device of the OCTAVE MULTIPLE TONE SYNTHESIZER family, producing 2 footage current outputs, for application in electronic musical instruments.

With this simple high integration component, used repetitively for each octave, the architecture of an electronic organ becomes:




The TMS36I5NS makes possible the introduction of substantial advantages in the electronic organ:

- achievement of modularity by matching the device count to the number of octaves in the keyboard
- major simplification of the architecture
- enhanced analog characteristics
- significant improvement of the reliability

KEY FEATURES

- Low cost P MOS technology
- 13 key input (octave organization)
- Internal tone generation (50% duty-cycle for RI107; 25% DUTY-cycle on the higher footage 12 tones for RI103).

If the gain stabilization is not needed, the STBOUT may be left open and the STBIN must be connected at $V_{SS}$.

A reset network is provided to synchronize many devices together and to allow the frequency counters (tos) enter their proper counting sequence. On the reset input RESIN there is a schmitt trigger to allow slow changing edges of the reset signal. The output of this shmitt trigger is available on RESOUT.

WARNING

In order to avoid that a mishandling of the PC Board might cause reliability problems associated with the internal circuitry, we suggest to connect the PIN4 and PIN 24 with an external resistor of .5 MΩ to $V_{SS}$ on the same PC board.

## DIVISIONAL FACTORS

The output frequencies are related to the input clock frequency through the following divisional factors:

| INPUT | OUT 8' | OUT 16' |
|---|---|---|
| K 1 | 478 | 956 |
| K 2 | 451* | 902 |
| K 3 | 426* | 852 |
| K 4 | 402* | 804 |
| K 5 | 379* | 758 |
| K 6 | 358* | 716 |
| K 7 | 338* | 676 |
| K 8 | 319* | 638 |
| K 9 | 301* | 602 |
| K10 | 284* | 568 |
| K11 | 268* | 536 |
| K12 | 253* | 506 |
| K13 | 239* | 478 |

* Duty cycles other than 50% (RI107) and 25% (RI103) available upon request.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Clock input low level pulse width | | 200 | | | ns |
| Clock input high level pulse width | | 200 | | | ns |
| Reset in low level | | | | -8 | V |
| Reset in high level | | -2.5 | | | V |
| K input level for 0% modulation index | | VDD | VDD | VDD | V |
| K input level for 100% modulation index | | | -1.8 | | V |
| Clock Out low level | R load $\geq$ 1 M | | | -8 | V |
| Clock Out high level | | -1 | | | V |
| Clock Out rise/fall | C load $\leq$ 30 pF | | | 150 | ns |
| Reset Out low level | R load $\geq$ 1 M | | | -9 | V |
| Reset Out high level | | -1 | | | V |
| STB Out/Footage Out bias voltage (See Fig.C) | | VDD-2 | VDD | VDD+2 | V |
| STB Out Current (See Fig.D) | STB Out at VDD<br>STB in Voltage=VDD | | 190 | | uA |
| Power Supply VDD | | -11 | | -16 | V |
| Power Consumption | All outputs open<br>Reset In = Low<br>Sustain Bias=VSS | | | 40 | mA |

NOTE: unused K inputs must be tied at Vss.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage VDD | VSS + .3V to VSS -20V |
| Input Voltage Range | VSS + .3V to VSS -20V |
| Storage Temperature | -55°C to +I50°C |
| Total Power Dissipation at (or below) 25°C Free-Air Temperature | I W |
| Operating Free-Air temperature Range | 0°C to 50°C |

## ELECTRICAL CHARACTERISTICS

At 25°C Free-Air Temperature VSS = OV, VDD = -I5V (Unless Otherwise Specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| STBIN Input Current (See Fig.A) | VIN=VDD | | 30 | | uA |
| K Input Impedance (See Fig.B) | VK=VDD, Pin2 at VDD<br>VK=VDD, Pin2 at VSS | 30<br>30 | 45<br>I000 | 60 | KΩ<br>MΩ |
| Input leakage current (any input except K inputs and PIN22) | VIN=VDD<br>All other Pins at VSS | | | I | uA |
| Clock input frequency | | 20 | | *2200 | KHz |
| Clock input rise/fall | | | | I50 | ns |
| Clock input high | | -I | | | V |
| Clock input low | | | | -7 | V |

*4.4Mhz available upon request

# TYPICAL CHARACTERISTICS

## STB IN CURRENT Vs STB IN VOLTAGE

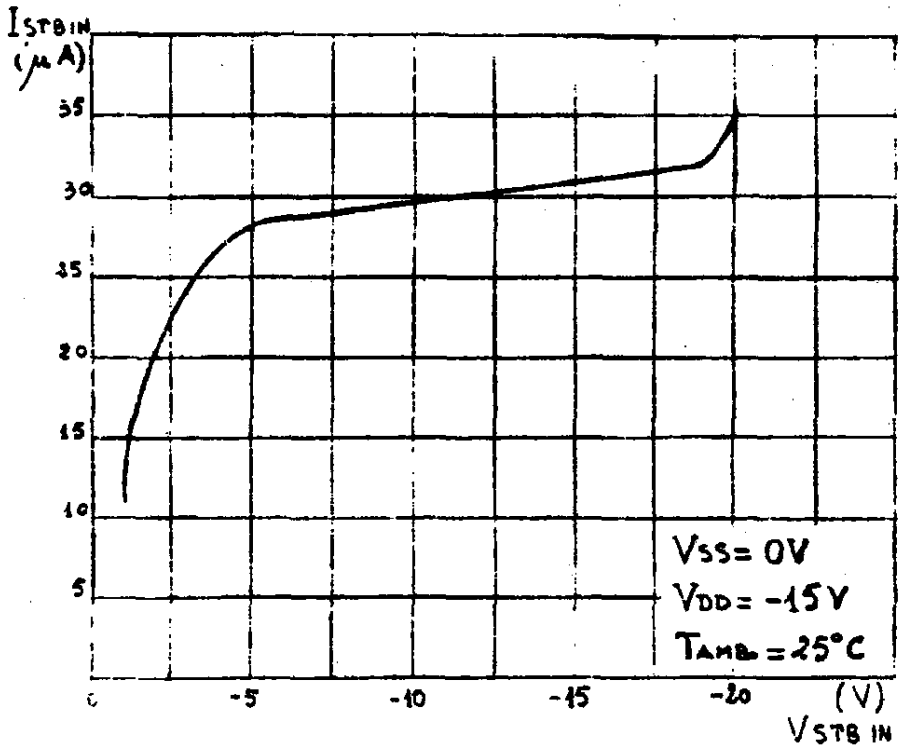



FIG. A

## K INPUTS CURRENT Vs K INPUTS VOLTAGE

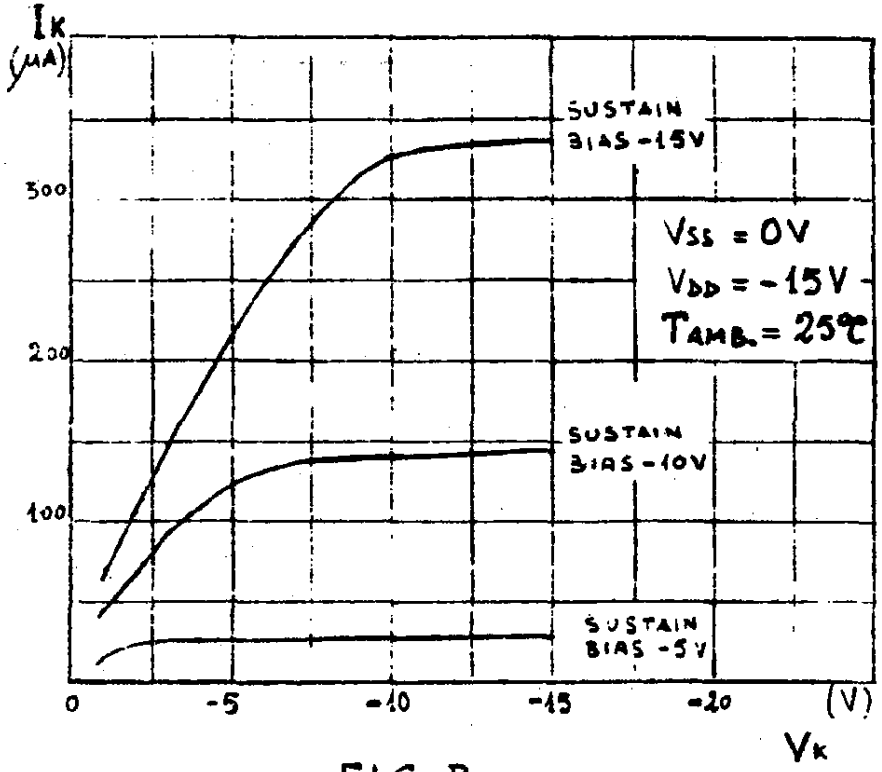



FIG. B

PIN 1 & PIN 24

NORMALIZED OUTPUT CURRENT
Vs
OUTPUT VOLTAGE

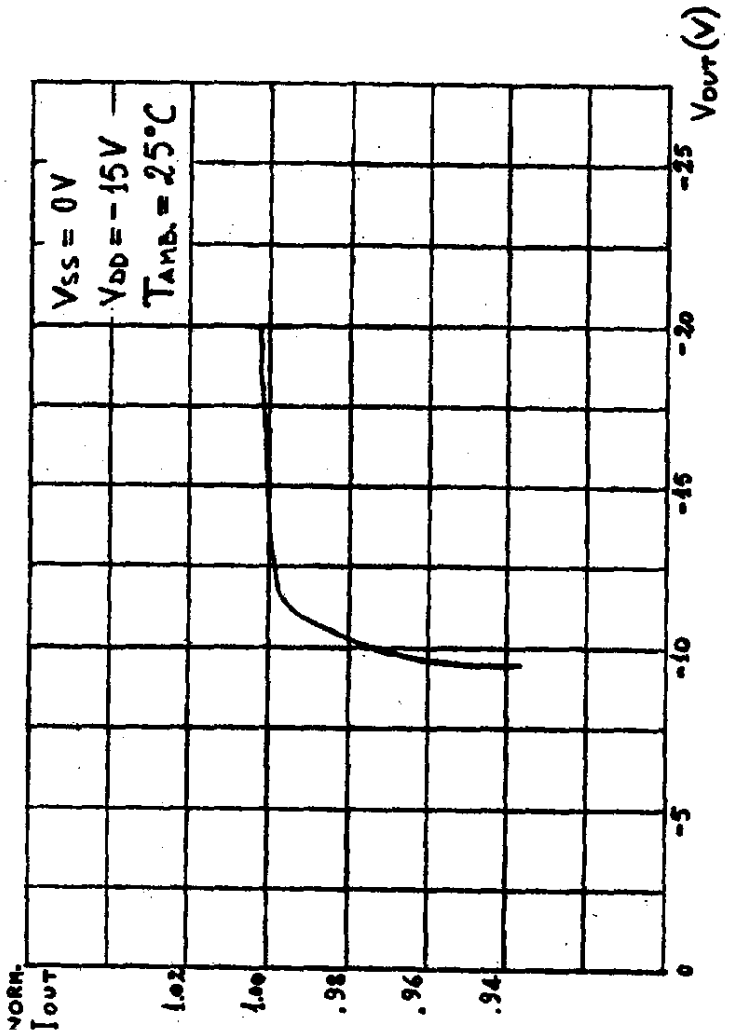



FIG. C

## TYPICAL CHARACTERISTICS

### STBOUT CURRENT Vs STBIN VOLTAGE

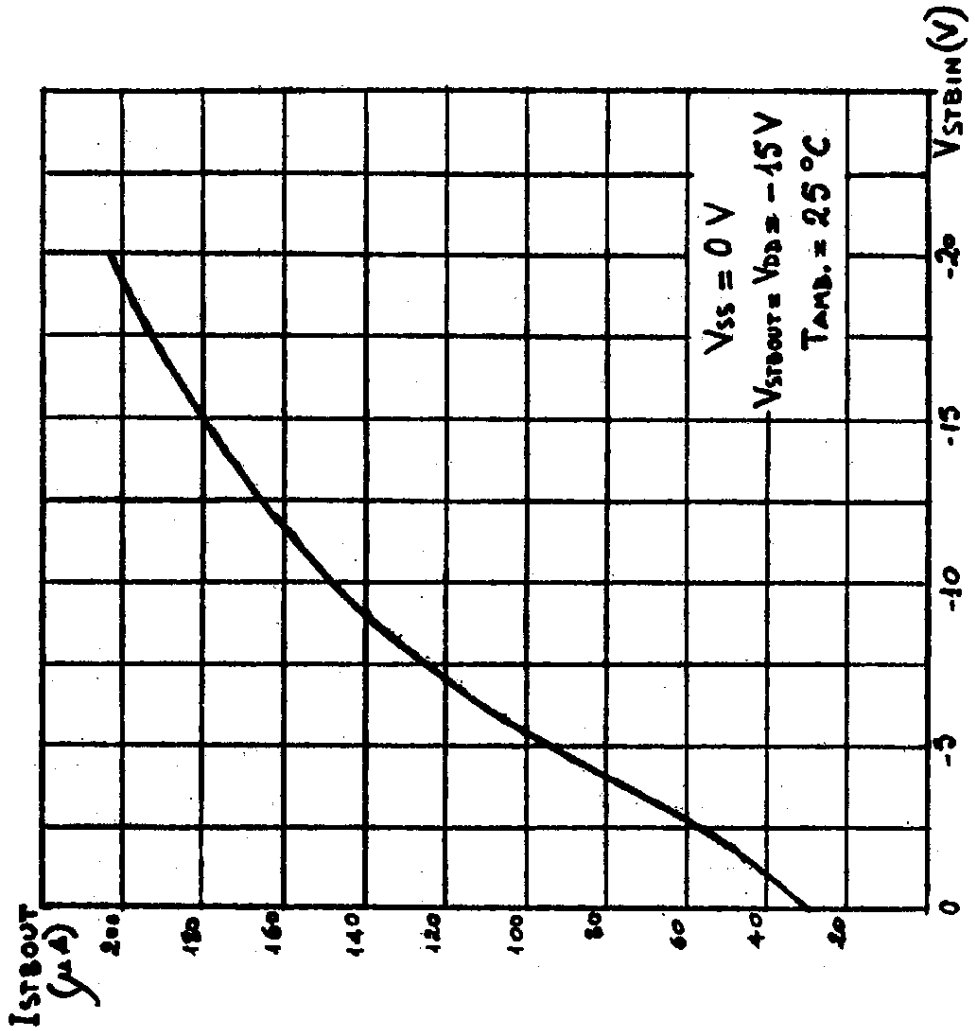
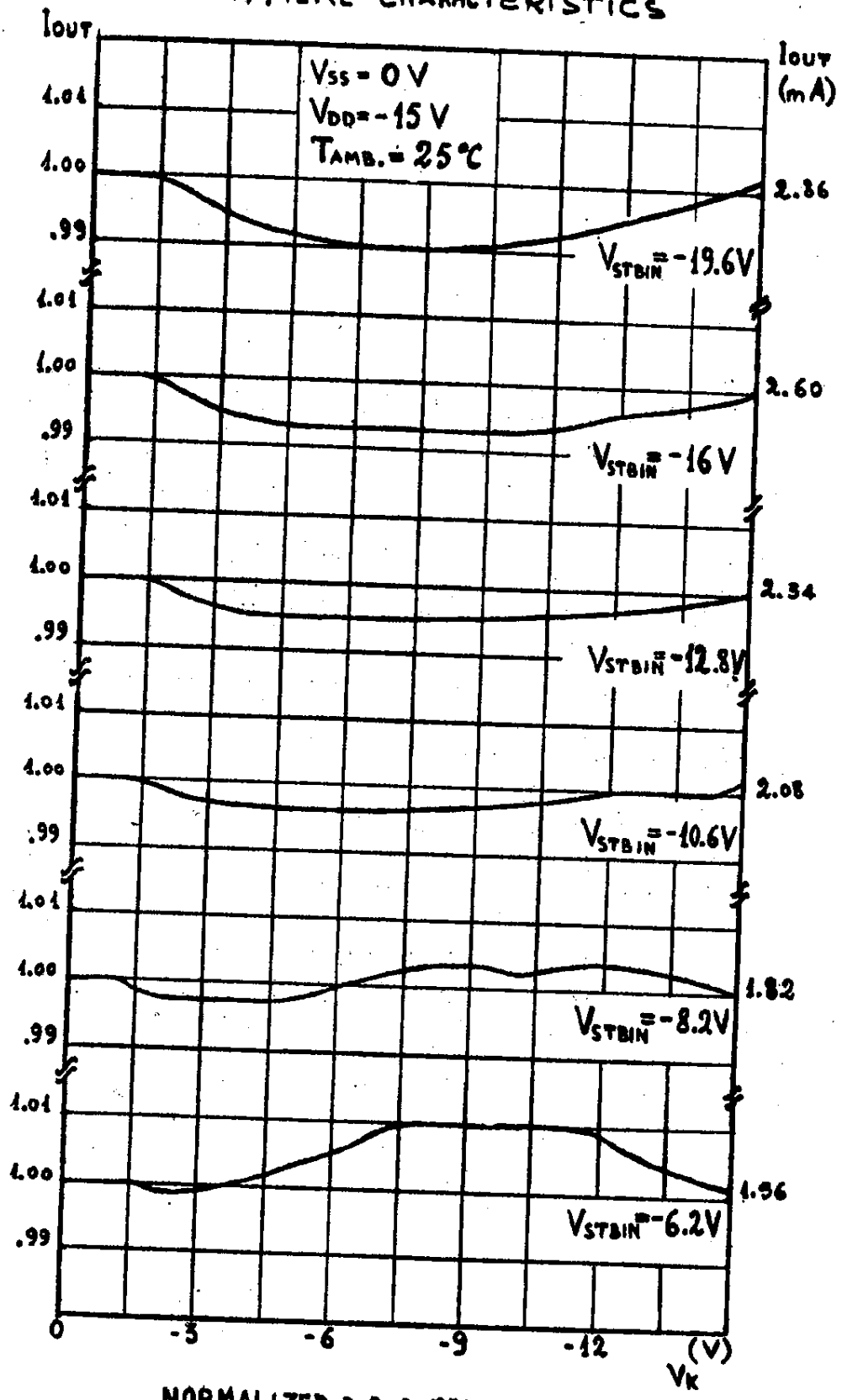



FIG. D

PIN 1 & PIN 24
TYPICAL CHARACTERISTICS




NORMALIZED D.C. OUTPUT CURRENTS
Vs
SINGLE K INPUT VOLTAGE

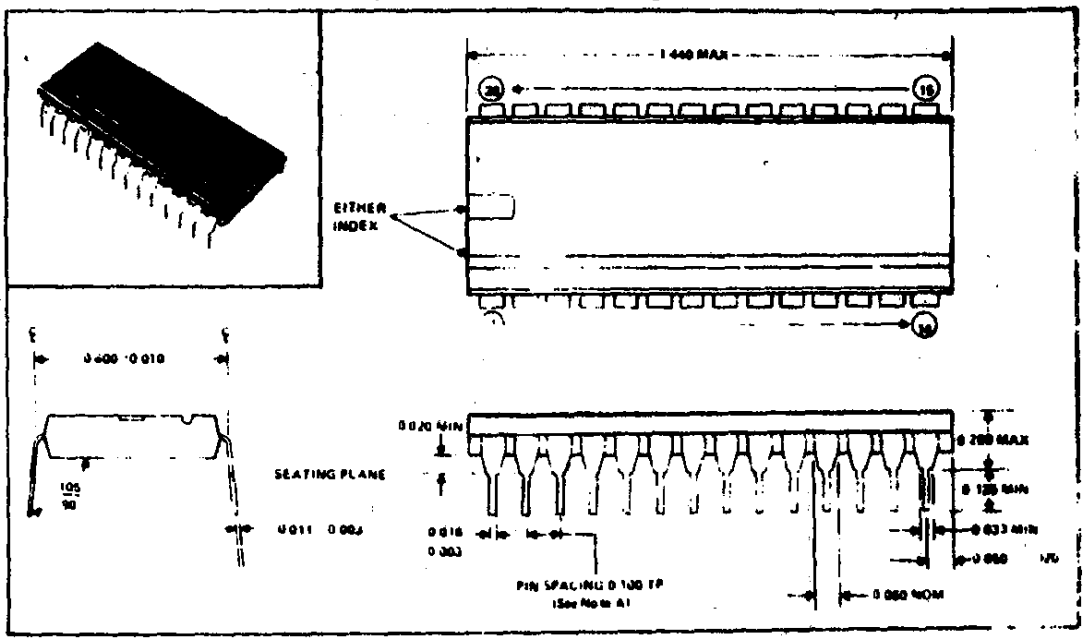
FIG. E

## PIN ASSIGNMENT

| PIN NBR | FUNCTION |
|---|---|
| 1 | NC |
| 2 | NC |
| 3 | 16' OUT |
| 4 | SUSTAIN BIAS |
| 5 | VSS |
| 6 | K 8 |
| 7 | K 9 |
| 8 | K 10 |
| 9 | K 11 |
| 10 | K 12 |
| 11 | K 13 |
| 12 | RESET OUT |
| 13 | CLOCK IN |
| 14 | VDD |
| 15 | CLOCK OUT |
| 16 | RESET IN |
| 17 | K 1 |
| 18 | K 2 |
| 19 | K 3 |
| 20 | K 4 |
| 21 | K 5 |
| 22 | K 6 |
| 23 | K 7 |
| 24 | STBIN† |
| 25 | STBOUT |
| 26 | 8' OUT |
| 27 | NC |
| 28 | NC |

# MECHANICAL CHARACTERISTICS

28-PIN PLASTIC DUAL-IN-LINE PACKAGE




NOTE A: Each pin centerline is located within 0.010 of its true longitudinal position.

B: All linear dimensions are in inches.