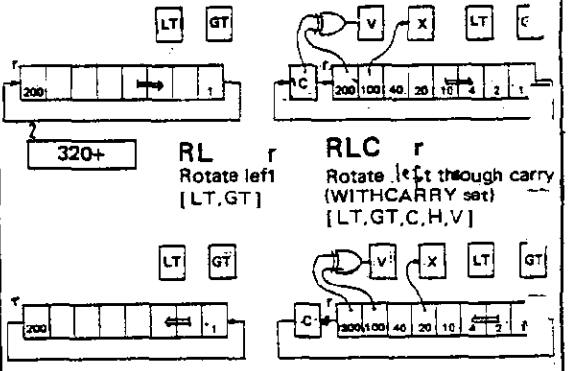
[Flags modified]

x y

| | | | |
|---|---|---|---|
| 0++ | **LOAD** Load x with y [LT,GT] | 2 (1) 0+ | A,r Register |
| | | 2 4+ n | r,#n Immediate |
| 300++ | **LOAD** Load y with x (store). LOAD #n,r does not exist LOAD r,A modified LOAD memory does not modify flags | 3 10+ ℓ'-2 | r, · + ℓ' Relative |
| | | 5 10+ 200+ℓ'-2 | r,@ · + ℓ' Relative indirect |
| 200++ | **ADD** Add x and y, result in x<br>**ADDC** Add carry if WITHCARRY set<br>[LT,GT,C,H,V] | 4 14+ p' a | r,m Absolute m' |
| 240++ | **SUB** Subtract with borrow if<br>**SUBB** WITHCARRY set<br>[LT,GT,C,H,V]<br>(add 2-s complement) | 6 14+ 200+p' a | r,@ m Absolute indirect 100000+m' |
| 100++ | **AND** Logical AND [LT,GT]<br>! AND A,A = WAIT | 4 14+ 140+p' a | A,(r)+m Indexed 60000+m' |
| 140++ | **OR** Logical OR [LT,GT] | 6 14+ 340+p' a | A,(r)+@m Indirect indexed 160000+m' |
| 40++ | **XDR** Exclusive OR [LT,GT] | 4 14+ 40+p' a | A,(+r)+m Pre-incrementing indexed 20000+m' |
| 340++ | **COMP** Compare arithmetic, logic if LOGICOMP set) [LT,GT] | 6 14+ 240+p' a | A,(+r)+@m Pre-incrementing indirect indexed 120000+m' |
| | | 4 14+ 100+p' a | A,(−r)+m Pre-decrementing indexed 40000+m' |
| | | 6 14+ 300+p' a | A,(−r)+@m Pre-decrementing indirect indexed 140000+m' |

| | | |
|---|---|---|
| 2 (1) 300 | **NDP** No operation [none] | |
| 100 | **WAIT** Wait for interrupt | |

| | | |
|---|---|---|
| 2 120+ | **RR** r Rotate right [LT,GT] | **RRC** r Rotate right though carry (WITHCARRY set) [LT,GT,C,H,V] |
| 2 320+ | **RL** r Rotate left [LT,GT] | **RLC** r Rotate left though carry (WITHCARRY set) [LT,GT,C,H,V] |



| | | |
|---|---|---|
| 3 364+ n | **TEST** r,#n Test bit [LT=NO,GT←o[ | r: 0 A, 1 B, 2 C, 3 D |
| 3 224+ | **DA** r [LT,GT] Decimal adjust Flag value does not corresoond to final result | |
| 3 124+ n | **LOAD** r,$n [LT,GT] | Read peripheral r data read in r |
| 3 324+ n | **LOAD** $n,r [none] | Write in peripher: data in r |
| 2 160 + | **LOAD** r,$DATA [LT,GT] | Read specially decoded peripheral |
| 2 360 + | **LOAD** $DATA,r [none] | Write in specially decoded peripheral |
| 2 60 + | **LOAD** r,$CTRL [LT,GT] | Read specially decoded peripheral |
| 2 260 + | **LOAD** $CTRL,r [none[ | Write in specially decoded peripheral |

| | | |
|---|---|---|
| 3 166 100 | **SET** [O] | **OUTPUT** |
| 164 100 | **CLR** [O] | **OUTPUT** |
| 164 40 | **ION** | CLR IOF |
| 166 40 | **IOF** | SET IOF |
| 164 7 | **CLR** [SP] | **STACK** |
| 167 20 | **SET** [B] | **BANK1** |
| 165 20 | **CLR** [B] | **BANK1** |

| | | |
|---|---|---|
| 3 167 10 | **SET** [W] | **WITHCARRY** |
| 165 10 | **CLR** [W] | **WITHCARRY** |
| 167 2 | **SET** [L] | **LOGICOMP** |
| 165 2 | **CLR** [L] | **LOGICOMP** |
| 167 1 | **SETC** [C] | SET CARRY |
| 165 1 | **CLRC** [C] | CLR CARRY |
| 167 4 | **SETV** [V] | SET OVERFLOW |
| 165 4 | **CLRV** [V] | CLR OVERFLOW |

| | | |
|---|---|---|
| 3 264 100 | **TEST** [LT=NO,GT←o] | **OUTPUT** |
| 264 200 | **TEST** | **INPUT** |
| 264 40 | **TEST** | IOF |
| 265 20 | **TEST** | BANK1 |
| 265 10 | **TEST** | WITHCARRY |
| 265 2 | **TEST** | LOGICOMP |
| 265 1 | **TEST** | CARRY |
| 265 4 | **TEST** | OVERFLOW |

| | | |
|---|---|---|
| 166 / n | OR | U,#n — Bit set |
| 167 / n | OR | L,#n — Bit set |
| 164 / n | BIC | U,#n — Bit clear |
| 165 / n | BIC | L,#n — Bit clear |
| 264 / n | TEST | U,#n — Test bit [LT=NO, GT←o] |
| 265 / n | TEST | L,#n — Test bit [LT=NO, GT←o] |
| 22 | LOAD | A,U [LT,GT] |
| 23 | LOAD | A,L [LT,GT] |
| 222 | LOAD | U,A [O, IOF, SP] |
| 223 | LOAD | L,A [LT,GT,H,B,W,V,L,C] |

Only on 2650-B (may never be produced)

| | | |
|---|---|---|
| 20 / p / a | LOAD | L,m — m [LT,GT,H,B,W,V,L,C] |
| 20 / 200+p / a | LOAD | L,@ m — 100000+m' [all] |
| 21 / p / a | LOAD | m,L — m [none] |
| 21 / 200+p / a | LOAD | @m,L — 100000+m [none] |

| | | |
|---|---|---|
| 30++ | JUMP,t | Jump if t true [none] |
| 70++ | CALL,t | Call if t true [SP] |

| | |
|---|---|
| 0+ / ℓ'−2 | ·+ℓ' |
| 0+ / 200+ℓ'−2 | @·+ℓ' |
| 4+ / p / a | m |
| 4+ / 200+p / a | @ m — 100000+m |

| t | | |
|---|---|---|
| 3 | | Unconditional |
| 0 | EQ | AO — Equal or equal to zero; All selected bits one after TEST instruction |
| 1 | GT | Greater than or strictly positive — GT=1 |
| 2 | LT | NO — Lower than or negative; Not all selected bits one — LT=1 |
| 200 | NE | Non equal or non equal to zero |
| 201 | LE | Lower or equal — GT=0 |
| 202 | GE | Greater or equal or positive — LT=0 |
| 100 | ANE | Register A non equal to zero |
| 101 | BNE | Register B non equal to zero |
| 102 | CNE | Register C non equal to zero |
| 103 | DNE | Register D non equal to zero |

| | | |
|---|---|---|
| 233+ | JUMP | Jump always [none] |
| 273+ | CALL | Call always [SP] |

| | |
|---|---|
| 0 / ℓ | 0+ℓ — Relative to location 0 |
| 0 / 200+ℓ | @0+ℓ |
| 4 / p / a | (D)+m — Indexed |
| 4 / 200+p / a | (D)+@m — Indirect indexed — 100000+m |

| | | |
|---|---|---|
| 24+ | RET,t | Return if t true [SP] |
| 64+ | RETION,t | Return and clear interrupt mask [SP,IOF] |

| t | | |
|---|---|---|
| 3 | | Unconditional |
| 0 | EQ | AO |
| 1 | GT | |
| 2 | LT | NO |

| | | |
|---|---|---|
| 330++ | INCJ,NE | Increment register r and jump if non equal to zero [none] |
| 370++ | DECJ,NE | Decrement register r and jump if non equal to zero [none] |

| | |
|---|---|
| 0+ / ℓ'−2 | r,·+ℓ' |
| 0+ / 200+ℓ'−2 | r,@·+ℓ' |
| 4+ / p / a | r,m |
| 4+ / 200+p / a | r,@ m — 100000+m |

r: 0 A, 1 B, 2 C, 3 D

# Common Assembly Language for Microprocessors REFERENCE CARD

# SIGNETICS 2650

## REGISTERS

A

| BANKØ | BANK1 |
|---|---|
| B | B' |
| C | C' |
| D | D' |

## U Flag and mode register

| | | |
|---|---|---|
| 200 | I | INPUT (Sense) |
| 100 | O | OUTPUT (Flag) |
| 40 | IOF | IOF (Interrupt mask bit) |
| 0-7 | SP | STACK pointer |

Return address stack

## L Flag and mode register

| | | |
|---|---|---|
| 200 | LT | Lower than |
| 100 | NO | Not all one |
| 40 | GT | Greater than |
| 20 | H | Half carry |
| 10 | B | BANK1 (second register bank) |
| 4 | W | WITHCARRY (with carry mode bit) |
| 2 | V | OVERFLOW |
| 1 | C | CARRY (carry and no borrow bit) |

Number of cycles per instruction

| | | |
|---|---|---|
| 330+ / 0 | INC | r [none] |
| 370+ / 0 | DEC | r [none] |
| 40 | CLR | A (LT←o, GT←o) |

r: 0 A, 1 B, 2 C, 3 D

Minimum cycle duration

| | |
|---|---|
| 2650 | 2.4 µs (1.25 Mhz clock) |
| 2650-A | |
| (2650-B) | |
| 2650 AI | 1.5 µs |

2650-B will have additional instructions and 1 cycle register to register transfer.

Addresses and data conventions

| | |
|---|---|
| m | 15 bit address |
| m' | 13 bit address in same chapter as PC |
| p | 7 bit page address (1 page = 256. locations) |
| p' | 5 bit page address in same chapter |
| a | 8 bit address in a page |
| ℓ' | 7 bit displacement in 2-s complement (6 bit + sign bit) 0 to 101 positive, 177 (−1) to 102 (−76) negative |
| n | 8 bit value (positive or signed) |

MEMORY ORGANISATION

| | |
|---|---|
| 0 | CHAPTER 0 — 32. pages |
| 20000 | CHAPTER 1 — $CTRL |
| 40000 | CHAPTER 2 |
| 60000 | CHAPTER 3 — $DATA |
| 77777 | |

IB instruction add 1-s complement plus one
SUBB instruction add 1-s complement plus CARRY
Carry is set if result is positive (8-bit logical numbers)

A instruction add a value depending on C(carry) and X(auxiliary carry)

| X | C | Added value Binary | Hexa | Octal |
|---|---|---|---|---|
| 0 | 0 | 1010 1010 | AA | 252 |
| 0 | 1 | 1010 0000 | A0 | 240 |
| 1 | 0 | 0000 1010 | 0A | 12 |
| 1 | 1 | 0000 0000 | 00 | 0 |

BCD addition:
```
ADD   r,#146 (octal)
ADD   r,ADDEND
DA    r
```

BCD subtraction:
```
SUB   r,SUBTRAHEND
DA    r
```

Interrupt sequence:
IOF (set interrupt mask bit)
First byte of CALL 0+ℓ' is forced internally
Intack reads second byte of instruction
(Jump to location 0—77 and 177700—17777 with possible indirection)

Reset : Start at 0 with interrupt on (IOF=Ø)

For information on compatible cross-assemblers on PDP-11 minicomputers and on large computers, write to LCD EPFL, Bellerive 16, CH 1007 Lausanne Switzerland

REV4, Sept 1977.