2K x 8
2048 x 8-BIT STATIC RAM

- **Fully Static Operation; No Clocks, Refresh or Latches**
- **EPROM Compatible Pinout**
- **Industry Standard 24-Pin Package**
- **Two Line Control, $\overline{CE}$ Controls Power-Down, $\overline{OE}$ Controls Output Buffers — Eliminates Bus Contention**
- **150 ns Maximum Access Time**
- **Auto Power-Down**

The Intel® 2K x 8 is a 16,384-bit static RAM organized as 2048 words by 8 bits. It employs fully static circuitry which eliminates the need for clocks, refresh, or address setup and hold times. The auto power-down feature cuts power consumption when the device is disabled.

The 24-pin industry standard pinout allows easy upgrades to 4K x 8 static RAMs and compatibility to the 2732 4K x 8 and 2764 8K x 8 EPROMs in 28-pin sites. The two line control simplifies decoding and eliminates any possibility of bus contention.

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	OUTPUT	POWER
H	X	X	NOT SELECT	HIGH Z	STANDBY
L	H	H	SELECTED	HIGH Z	ACTIVE
L	H	L	READ	ACTIVE	ACTIVE
L	L	X	WRITE	HIGH Z	ACTIVE

PIN NAMES

A_0—A_{10}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
D_0—D_7	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

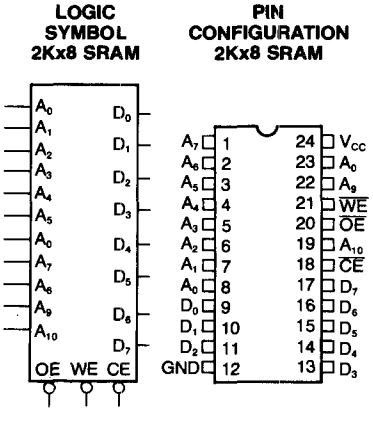


Figure 1. 2K x 8 Pin Diagram

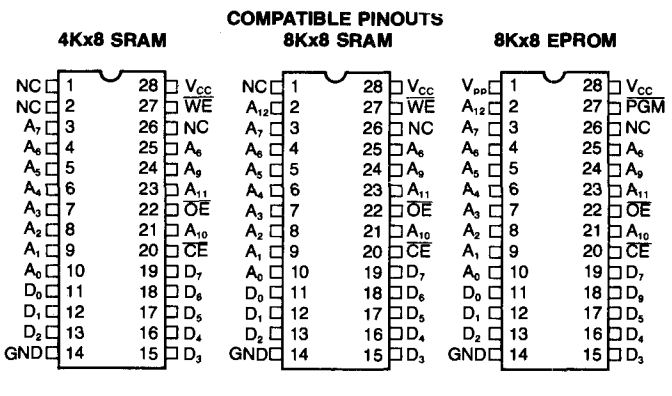


Figure 2. Compatible Pinouts

4K x 8
4096 x 8-BIT STATIC RAM

- **Fully Static Operation; No Clocks, Refresh or Latches**
- **EPROM Compatible JEDEC Standard Pinout**
- **2764 Compatible 28-Pin Package — Allows Easy Upgrade To 8K x 8 SRAM Without Jumpers**
- **Two Line Control, $\overline{CE}$ Controls Power-Down, $\overline{OE}$ Controls Output Buffers — Eliminates Bus Contention**
- **150 ns Maximum Access Time**
- **Auto Power-Down**

The Intel® 4K x 8 is a 32,768-bit static RAM organized as 4096 words by 8 bits. It employs fully static circuitry which eliminates the need for clocks, refresh, or address setup and hold times. The auto power-down feature cuts power consumption when the device is disabled.

The 28-pin JEDEC standard pinout allows easy upgrades to 8K x 8 static RAMs and compatibility to the 2732 4K x 8 and 2764 8K x 8 EPROMs — without jumpers. The two line control simplifies decoding and eliminates any possibility of bus contention.

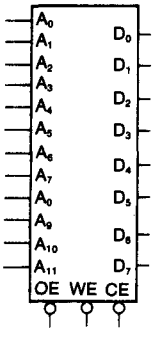
TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	OUTPUT	POWER
H	X	X	NOT SELECT	HIGH Z	STANDBY
L	H	H	SELECTED	HIGH Z	ACTIVE
L	H	L	READ	ACTIVE	ACTIVE
L	L	X	WRITE	HIGH Z	ACTIVE

PIN NAMES

A_0—A_{11}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
D_0—D_7	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

LOGIC SYMBOL 4K x 8



PIN CONFIGURATION 4Kx8 SRAM

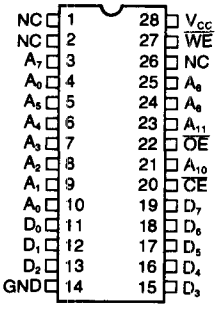
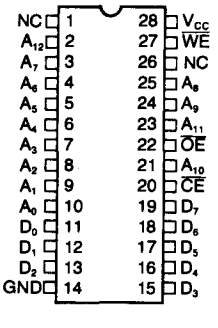


Figure 1. 4K x 8-Pin Diagram

COMPATIBLE PINOUTS

8Kx8 SRAM



8Kx8 EPROM

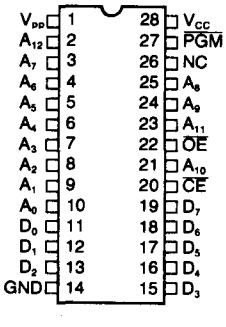


Figure 2. Compatible Pinouts

2732
32K (4K x 8) UV ERASABLE PROM

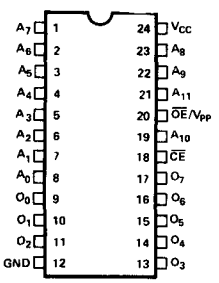
- **Fast Access Time:**
  - **— 390 ns Max. 2732-4**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Industry Standard Pinout — JEDEC Approved**
- **Pin Compatible to Intel's EPROM Family: 2716, 2732A, 2764**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  - **— 150 mA Max. Active Current**
  - **— 35 mA Max Standby Current**
- **Single +5V ± 5% Power Supply**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. The 2732 family with an access time up to 390 ns enhances microprocessor system performance. This family, in conjunction with the 250 ns 2732A family, solves the problem of WAIT states due to slow memories.

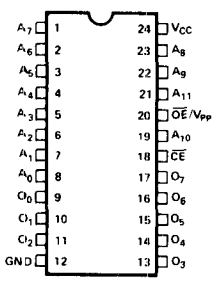
An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150 mA, while the maximum standby current is only 35 mA, a 75% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

2732 PIN CONFIGURATION



2732A PIN CONFIGURATION



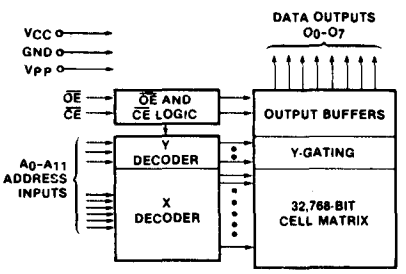
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +125°C
All Input or Output Voltages with
Respect to Ground ..... +6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

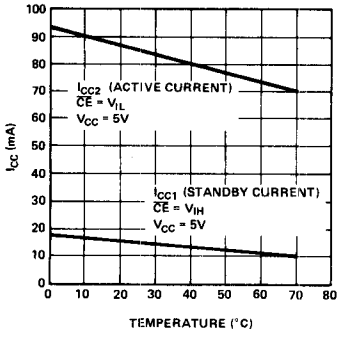
READ OPERATION

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	μA	V_{IN} = 5.25V
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{CC1}	V_{CC} Current (Standby)		15	35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400μA

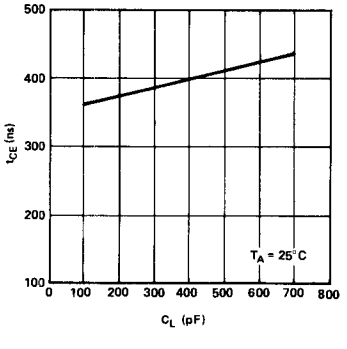
Note: 1. Typical values are for T_A = 25°C and nominal supply voltages.

TYPICAL CHARACTERISTICS

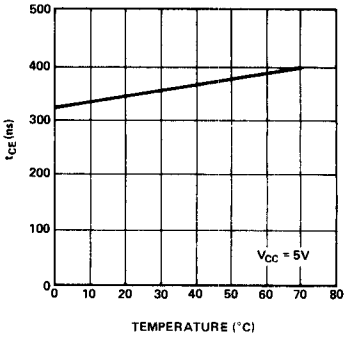
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	2732-4 Limits (ns)		2732 Limits (ns)		2732-6 Limits (ns)		Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		390		450		550	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		390		450		550	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

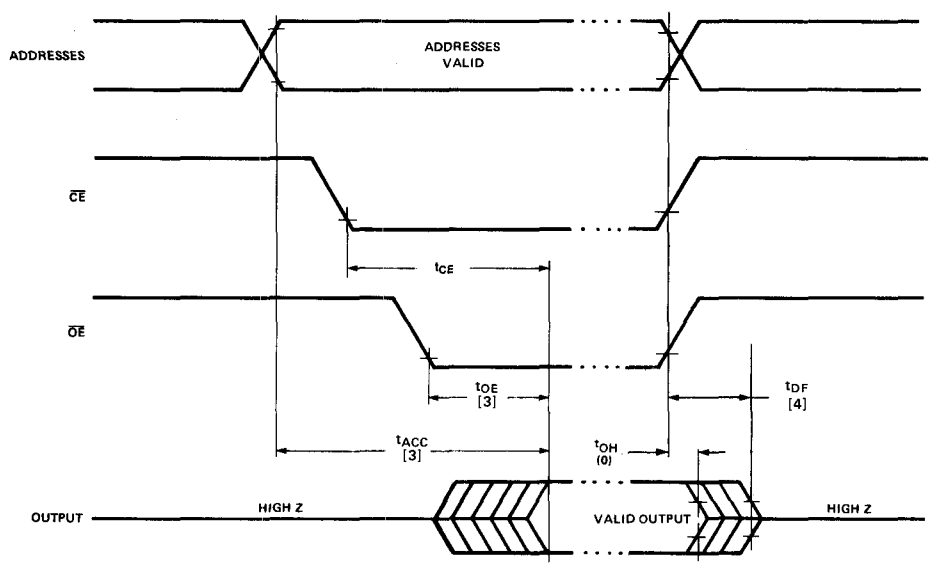
CAPACITANCE [1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS [2]



NOTES:
1. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
2. ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE NSEC UNLESS OTHERWISE SPECIFIED.
3. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
4. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog) for the 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (,). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2732 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

TABLE 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2732 has a standby mode which reduces the active power current by 75%, from 150mA to 35mA. The 2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING (See Programming Instruction Section for Waveforms.)

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.