PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

DESCRIPTION

The Signetics 2637 Universal Video Interface (UVI), using a new design approach, enables a microprocessor based system to be interfaced more efficiently with a color or black and white television receiver or monitor. For the first time, the 2637 UVI combines an object oriented approach with character generation (alphanumerics or other displayable forms) plus RAM-mapped color graphics.

The UVI's primary use is in microprocessor controlled home computers or game systems, however, it may also be used in other applications where the display of alphanumeric and graphics data is desired. In particular, the UVI has been designed to require a minimum of support components thereby allowing a system configuration that is optimized for the user's needs.

The UVI reads data and operational commands from a memory and produces video signals that result in the generation of alphanumeric or graphics color TV displays. Many of the common display circuits have been incorporated in a single chip, including:

- Analog to digital converters which accept potentiometer inputs
- Alphanumeric and special character generators
- Moving object circuits
- Audio signal generators

With the 2637, a typical system configuration consists of a UVI, a 2616/2632 ROM, a 2622 (NTSC) or 2621 (PAL) Universal Sync Generator (USG), a 6650 series microprocessor, four 2112 RAMs, and video summing circuitry. Additional UVIs, Programmable Video Interfaces (PVIs), as well as random logic can be interfaced to enhance game or system complexity.

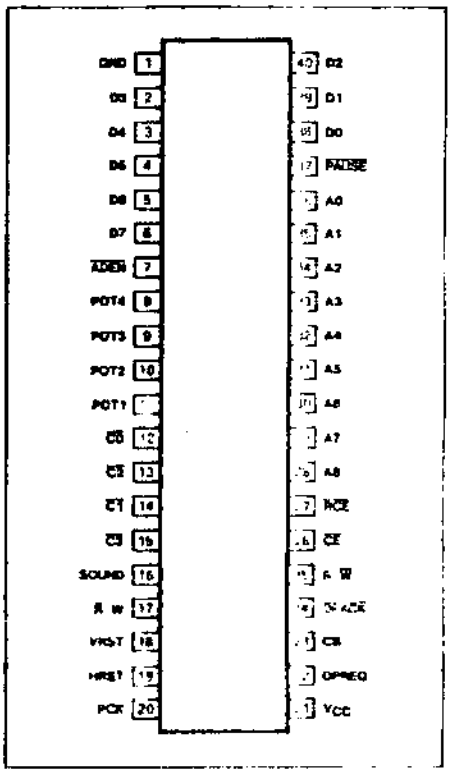
FEATURES

- **Four general purpose, RAM-resident objects**
- **280nsec object resolution**
- **Object size and position under program control**
- **Programmable multi-level sound and noise generators**
- **16 characters per display row**
- **13 or 26 character rows per screen**
- **40 alphanumeric characters**
- **16 background characters**
- **8 program definable characters**
- **64 graphics characters**
- **8 programmable color codes**
- **Chip enable outputs for I/O logic**
- **I/O facilities for switch scanning and potentiometer (RC) inputs**
- **Operates with both U.S. and European standards**
- **Single +5 volt power supply**
- **Forty-pin package**

APPLICATIONS

- **Video games**
- **Home computers**
- **Communications terminals**
- **Educational systems**
- **Process control displays**
- **Medical electronics**

PIN CONFIGURATION



ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%, T_A = 0°C to 55°C
Ceramic DIP	2637I
Plastic DIP	2637N

UVI FUNCTIONAL DESCRIPTION

The 2637 UVI is a bus oriented device with address and data busses controlling the flow of data between the user's system and the UVI (see block diagram). Both the address and data busses are bidirectional.

The basic clock frequency and the horizontal and vertical reset signals to the UVI drive vertical and horizontal counters. The two counters provide the UVI with a Cartesian coordinate representation of the television screen, i.e., each counter pair describes a unique point on the screen. Typically these clock and reset signals are provided by a universal sync generator circuit.

A/D Block

The A/D Block converts the analog potentiometer position information into binary data which can be read by the system's CPU. Only two of the four potentiometers are active at any given time.

Address Block

The address block provides chip enable outputs for external RAMs and I/O buffers.

Sound Block

The sound block is a multi-level square wave generator sending out pulses at a user programmable audio frequency. Random noise is also generated and can be mixed with the audio frequency for simulating crowd noise, explosions, etc.

Internal Status Block

The internal status block accumulates status information which can be read by the CPU; for example, collisions.

Color Mux System

The color multiplexer generates the color codes for characters, objects, and screen.

ROM Character Generator

The ROM character generator stores the character fonts.

RAM

The 64 bytes of RAM stores eight programmable character/object fonts.

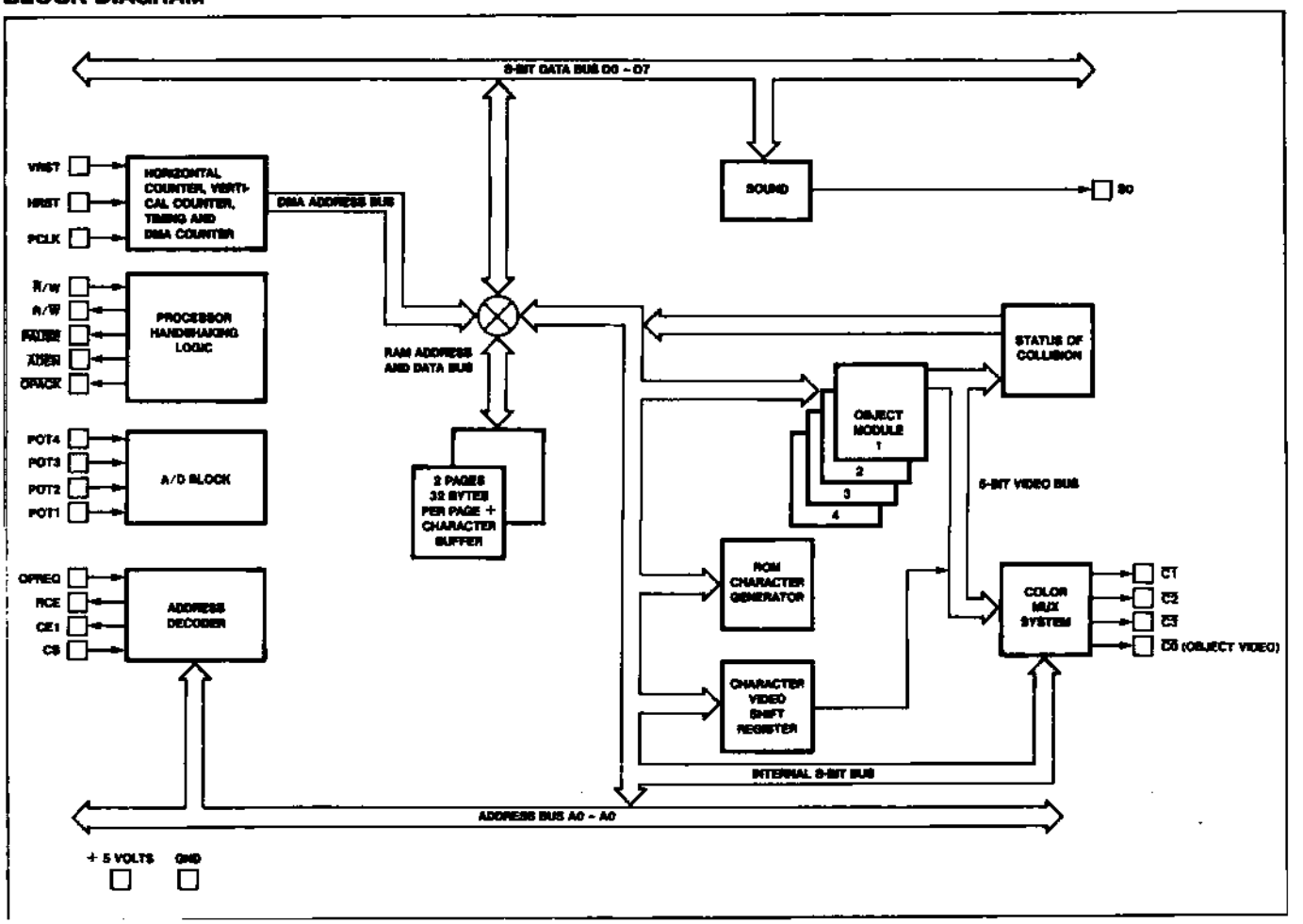
PRELIMINARY SPECIFICATION

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
A0-A8	36-28	I/O	**Address Bus:** 9-bit bidirectional address bus.
D0-D7	2-6, 38-40	I/O	**Data Bus:** 8-bit bidirectional data bus.
OPREQ	22	I	**Operation Request:** When high, all signals from the CPU must be valid.
R/W	17	I	**Read/Write:** Specifies direction of data transfer with respect to the CPU. Read when low, write when high.
$\overline{DPACK}$	24	O	**Operation Acknowledge:** The UVI pulls this signal to ground when it is ready to service the CPU.
$\overline{PAUSE}$	37	O	**CPU Pause:** Active low DMA request from the UVI to the CPU. The CPU lowers this signal when it wants to access the display RAM.
$\overline{ADEN}$	7	O	**Address and Data Bus Enable:** This output is high when the UVI performs DMA operations. It is low when the CPU is granted control of the busses.
CS	23	I	**Chip Select:** Active high input which controls UVI accesses.
PCK	20	I	**Position Clock:** Generated by the USG to synchronize the UVI's internal functions (3.58MHz, 227 pulses/line).
C1, C2, C3	14,13,15	O	**Color 1, Color 2, Color 3:** Outputs denoting the color to be displayed.
VRST	18	I	**Vertical Reset:** The USG provides the signal to synchronize the UVI's vertical counter.
HRST	19	I	**Horizontal Reset:** This signal is provided by the USG to synchronize the UVI's horizontal count chain.
$\overline{RCE}$	27	O	**RAM Chip Enable:** This output is low when the CPU addresses the display RAM.
R/$\overline{W}$	25	O	**RAM Read/Write:** Signal which indicates whether the UVI is reading from or writing into the display RAM. Read when high, write when low.
POT1-POT4	11-8	I	**Potentiometer Inputs:** These pins connect to external variable RC networks for A-D conversion.
SOUND	16	O	**Digital Sound:** An audio frequency square wave output generated under program control.
$\overline{OD}$	12	O	**Object Video:** This output goes low when the UVI is presenting object information. It serves as the fourth color output.
V_{CC}	21	I	**Power Supply:** +5V ±5%
GND	1	I	**Ground:** 0V reference ground.
$\overline{CE}$	26	O	**I/O Chip Enable:** Active low output to select an I/O device.

PRELIMINARY SPECIFICATION

BLOCK DIAGRAM



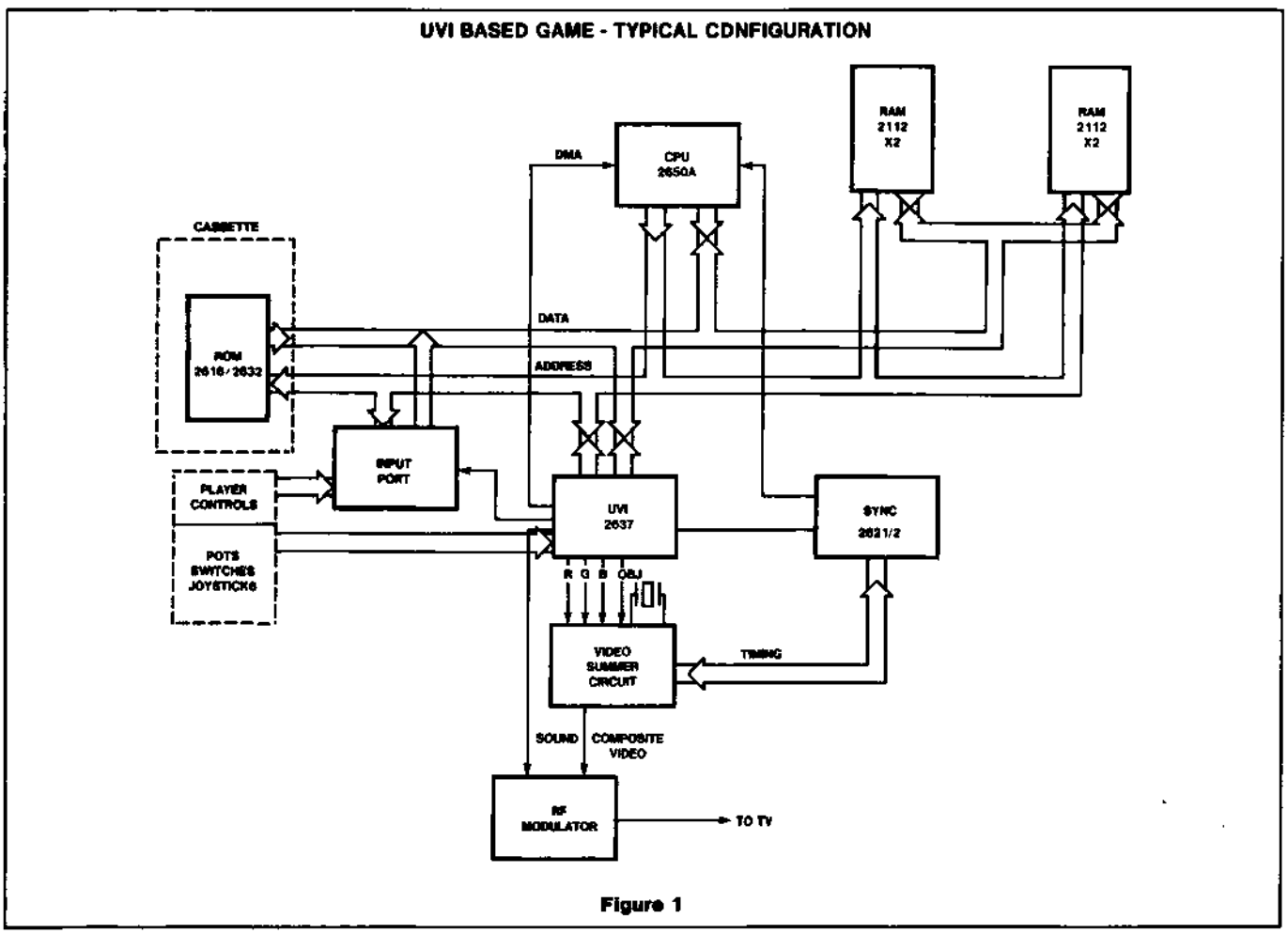

UVI BASED GAME - TYPICAL CONFIGURATION
RAM 2112 X2
RAM 2112 X2
DMA
CPU 2650A
CASSETTE
ROM 2616 / 2632
DATA
ADDRESS
INPUT PORT
PLAYER CONTROLS
POTS SWITCHES JOYSTICKS
UVI 2637
SYNC 2621/2
R G B OBJ
VIDEO SUMMER CIRCUIT
TIMING
SOUND
COMPOSITE VIDEO
RF MODULATOR
TO TV

Figure 1

TYPICAL UVI BASED HOME COMPUTER

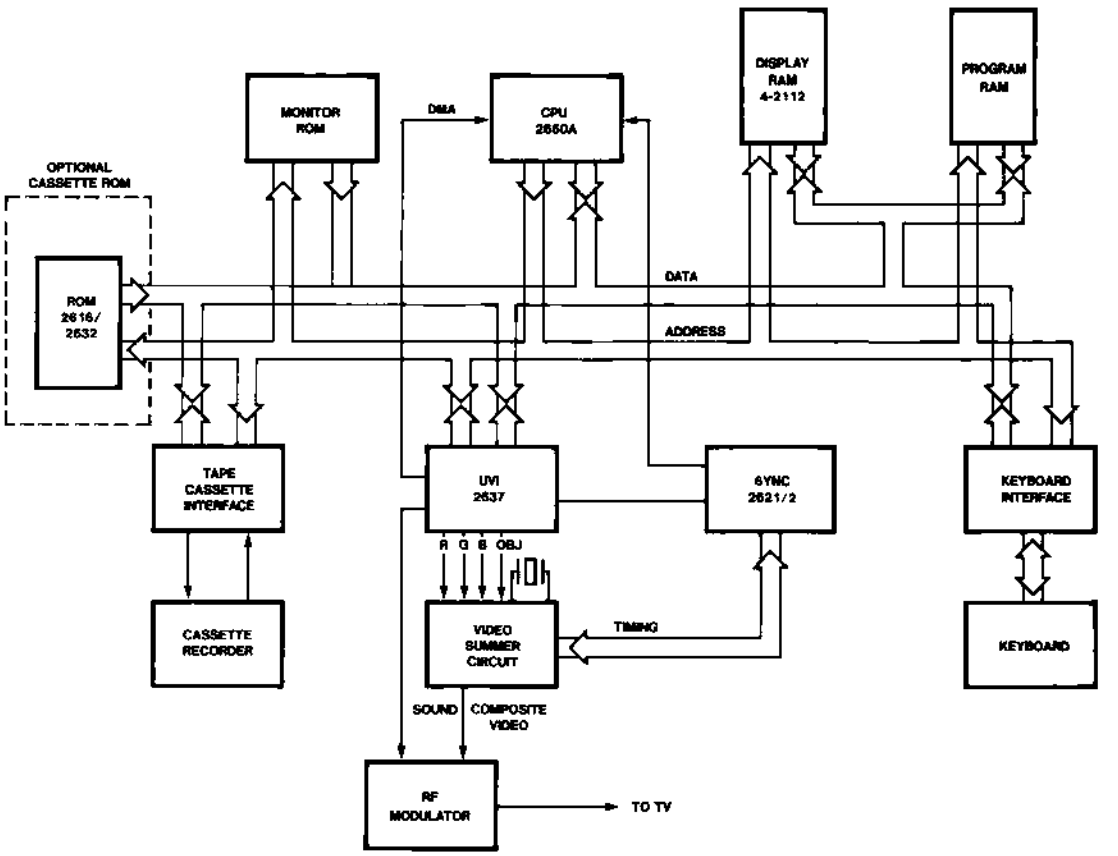


Figure 2

EXTERNAL MEMORY MAP WITH ADDRESS LINE 12 USED AS CS

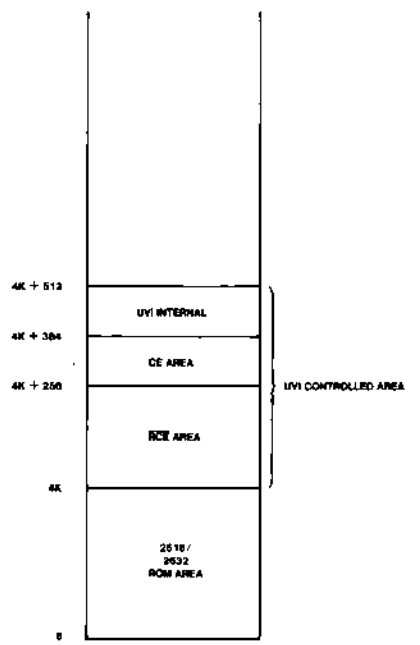


Figure 3

EXTERNAL RAM MEMORY MAP

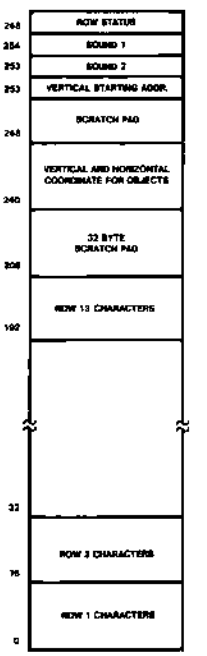


Figure 4

MEMORY MAP – RAM

ADDRESS	7	6	5	4	3	2	1	0	TYPE OF UVI ACCESS	EXPLANATION
H'FF'	←→ 7 →				R_3 DMA	R_2	R_1 Status	R_0	Write	R = ROW 15 implies beginning of DMA, 13 indicates end of DMA
H'FE'	Character shift SH_2	SH_1	SH_0	RNG EN	FEN	Sound Loudness LS_2	LS_1	LS_0	Read	SH = no. of bits of delay for the row of characters RNG = 1 enables random noise to the sound output FEN = 1 enables the frequency counter to the sound output. LS specifies 1 of 8 levels of loudness
H'FD'	M	N_8	N_5	N_4	N_3	N_2	N_1	N_0	Read	M = color mode bit N = frequency counter terminal count.
H'FC'	$\overline{V}$ OFFSET								Read	$\overline{V}$ OFFSET = the complement of the number of lines from the trailing edge of vertical drive to start character display
H'F7'	Horizontal coordinate of object 4								Read	Coordinates of the four object images
H'F8'	Vertical coordinate of object 4									
H'F5'	Horizontal coordinate of object 3									
H'F4'	Vertical coordinate of object 3									
H'F3'	Horizontal coordinate of object 2									
H'F2'	Vertical coordinate of object 2									
H'F1'	Horizontal coordinate of object 1									
H'F0'	Vertical coordinate of object 1									

Figure 5

External Switch I/O

Switches can be addressed through the chip enable (CE) output in combination with the address bus. A typical 8 or 16-switch configuration can be accommodated by using a 74257 (tri-statable 8 to 4 multiplexer) or a 74LS251 (tri-statable 8 to 1 multiplexer).

Internal Organization

The UVI's internal logic blocks perform the following algorithms:

- Determines shape, color, position, and size of four objects
- Generates alphanumeric character video
- Produces multi-level sound
- Detects inter-object and object-background collision
- Converts selected potentiometer inputs to 8-bit digital values.

Figure 8 is a UVI memory map and figure 7 is an expansion of the I/O, sound, color, status and control sector.

CHARACTER VIDEO

The UVI presents 13 rows of 16 characters each to the TV screen (see figure 8). The characters are accessed from the external 2112, and decoded for identification of each

MEMORY MAP OF UVI INTERNAL—UPPER SECTOR

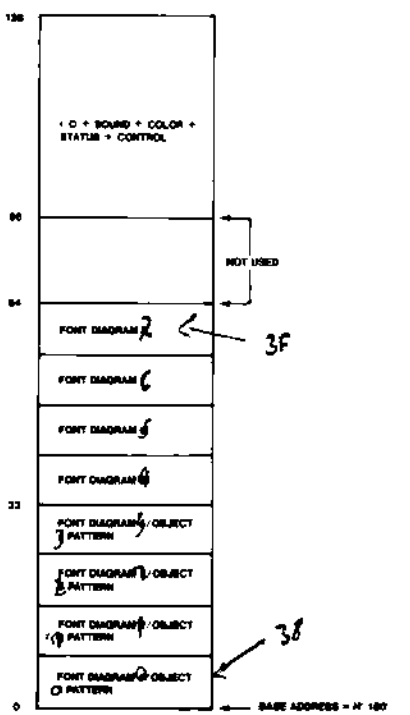


Figure 6

PRELIMINARY SPECIFICATION

MEMORY MAP OF UVI INTERNAL

A8–A0 ADDRESS	7	6	5	4	3	2	1	0	ACCESS TYPE	DESCRIPTION
1FF	MUX ↓ A/D Potentiometer 1/3								Read	During VRST: Returns value of A/D counter on POT1 or POT3 inputs. Range = H'00'–H'FE'. During $\overline{VRST}$: Returns value H'FF'.
1FE	A/D Potentiometer 2/4								Read	Same as above for POT2 or POT4 inputs
1FD	1	1	I_{34}	I_{24}	I_{23}	I_{14}	I_{13}	I_{12}	Read	I_{ij} – Intercollision status between objects i and j. The bits are reset on collision and set by reading or the trailing edge of VRST. (I_{ij} = 0) — collision
1FC	1	1	1	1	O_{4c}	O_{3c}	O_{2c}	O_{1c}	Read	O_{ic} – Collision status between object i and any character. The bits are reset on collision and set by reading or the trailing edge of VRST. (O_{ij} = 0) — collision
1FB	SZ_1	SZ_2	C_{11}	C_{12}	C_{13}	C_{21}	C_{22}	C_{23}	Write	C_{ij} – Color assignment of object i to color output C_j
1FA	SZ_3	SZ_4	C_{31}	C_{32}	C_{33}	C_{41}	C_{42}	C_{43}	Write	SZ_i – Size of object i. (SZ_i = 0) — object i size 8 clocks X 16 lines (SZ_i = 1) — object i size 8 clocks X 8 lines
1F9	SZ_c	P	C_{c1}	C_{c2}	C_{c3}	C_{s1}	C_{s2}	C_{s3}	Write	C_{cj} – Character color assignment to color outputs C_j. C_{sj} – Screen color assignment to color output C_j. SZ_c – Size of characters (SZ_c = 0) — character size 8 clocks X 16 lines (SZ_c = 0) — character size 8 clocks X 8 lines P – Potentiometer input mux control. (P = 0) — Inputs POT1, POT2, drive A/D at (1FF), (1FE) (P = 1) — Inputs POT3, POT4, drive A/D at (1FF), (1FE)
1F8	GM	REF	$C_{c'1}$	$C_{c'2}$	$C_{c'3}$	$C_{s'1}$	$C_{s'2}$	$C_{s'3}$	Write	$C_{c'j}$ – Alternate character color assign. $C_{a'j}$ – Alternate screen color assignment for character display area REF – Refresh mode. When set, the entire character field will be displayed twice, contiguously. GM – Graphics mode. When set/reset, forces/terminates the character graphics display mode at the beginning of each horizontal scan line.

Figure 7

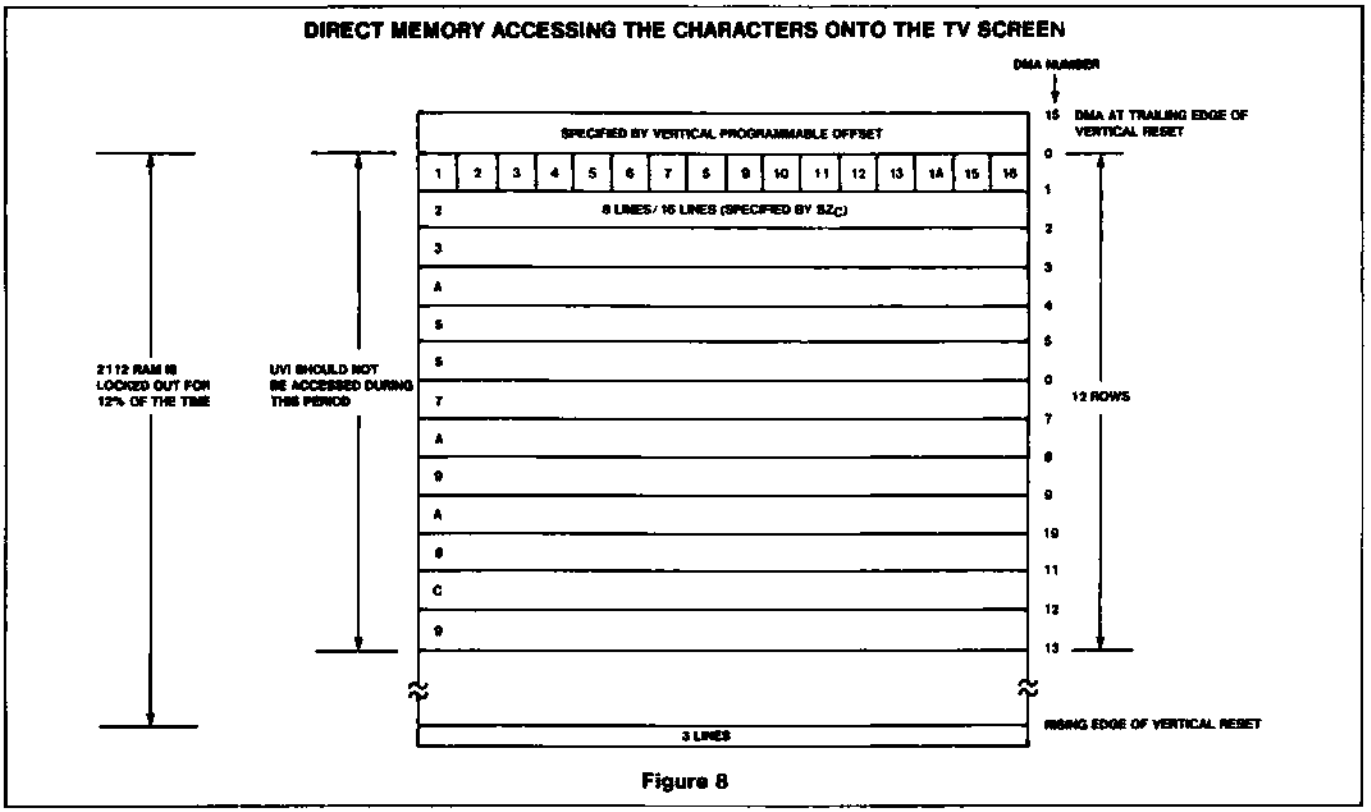


Figure 8

character. D5 through D0 represent the character code; D7 through D6 are the character color code.

Character Address

For any column x and row y on the screen, the external RAM address equals (y−1) × 16 + (x−1), e.g., the RAM address for row 1, column 1 equals (1−1) × 16 + (1−1) = 0.

Character DMA

There are 15 DMAs per frame numbered: 15, 0, 1, 2, 3, . . . 13, (see figure 8). Each DMA is preceded by a PAUSE request and tri-stating of the microprocessor bus after 60μsec. Then DMA is started for one TV scan line.

Address 255, 254 and 253 of the external RAM will be accessed for all DMA numbers. During each DMA access, the UVI will write the DMA number into external RAM at address location 255. The characters will be accessed from DMA 0 through 12 (screen space). The character codes are stored in a 16-character buffer and will continue to be displayed for the rest of the character lines. The vertical and horizontal coordinates of the four objects and vertical offset will be accessed at DMA 15. During the screen space, the 2650 should not access the UVI as the internal data bus is busy servicing the display.

The character video is shifted out 66 clocks after the rising edge of the horizontal reset. The character video shifting can be delayed up to 7 clocks by programming the SH field in location 254 of the external RAM (see figure 5). This provides horizontal scrolling on a row by row basis.

Character Color

Character color can be specified by mode 0 and mode 1 (for board games) operation. Mode is specified by the M bit (location 253) in external RAM.

1. M = 0 specifies mode 0

Font Video	C1	C2	C3
1	B7	B6	Cc3
0	C_{B1}	C_{B2}	C_{B3}

2. M = 1 specifies mode 1

Font Video	B7	B6	C1	C2	C3
1	X	1	C_{C1}	C_{C2}	C_{C3}
1	X	0	$C_{C'1}$	$C_{B'2}$	$C_{C'3}$
0	1	X	C_{B1}	C_{B2}	C_{B3}
0	0	X	$C_{B'1}$	$C_{B'2}$	$C_{B'3}$

X = don't care

Character Set

The UVI character set consists of 40 mask programmable characters (8 × 6), 16 fixed background characters and 8 dynamically programmable characters. Figure 9 illustrates the font diagrams of all fixed background characters. Figure 10 shows a standard character set.

The variable character font is stored in UVI RAM and can be changed during the vertical reset period.

Refresh Mode

When the REF bit at UVI address H'1F8' is set, the UVI will cycle through the character display a second time. In this mode, a total of 416 characters will be displayed. Two additional 2112 RAMs can be added to hold the second 208 characters.

Character Address—Refresh Mode

For any column X and row Y on the screen, the external RAM address is:

ADD = (y−1) × 16 + (x−1) for $1 \leq Y \leq 13$

ADD = 256 + (y−14) × 16 + (x−1) for $14 \geq Y \geq 26$

UVI BACKGROUND CHARACTER SET

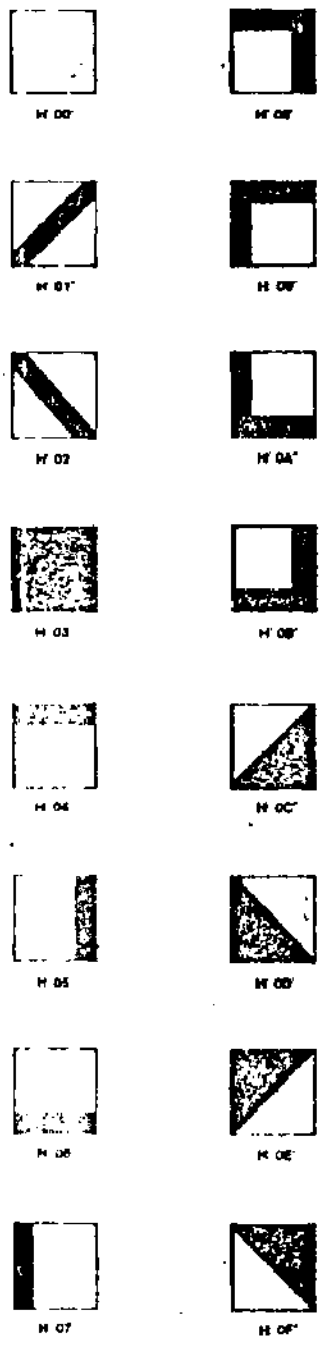


Figure 9

STANDARD UVI CHARACTER SET

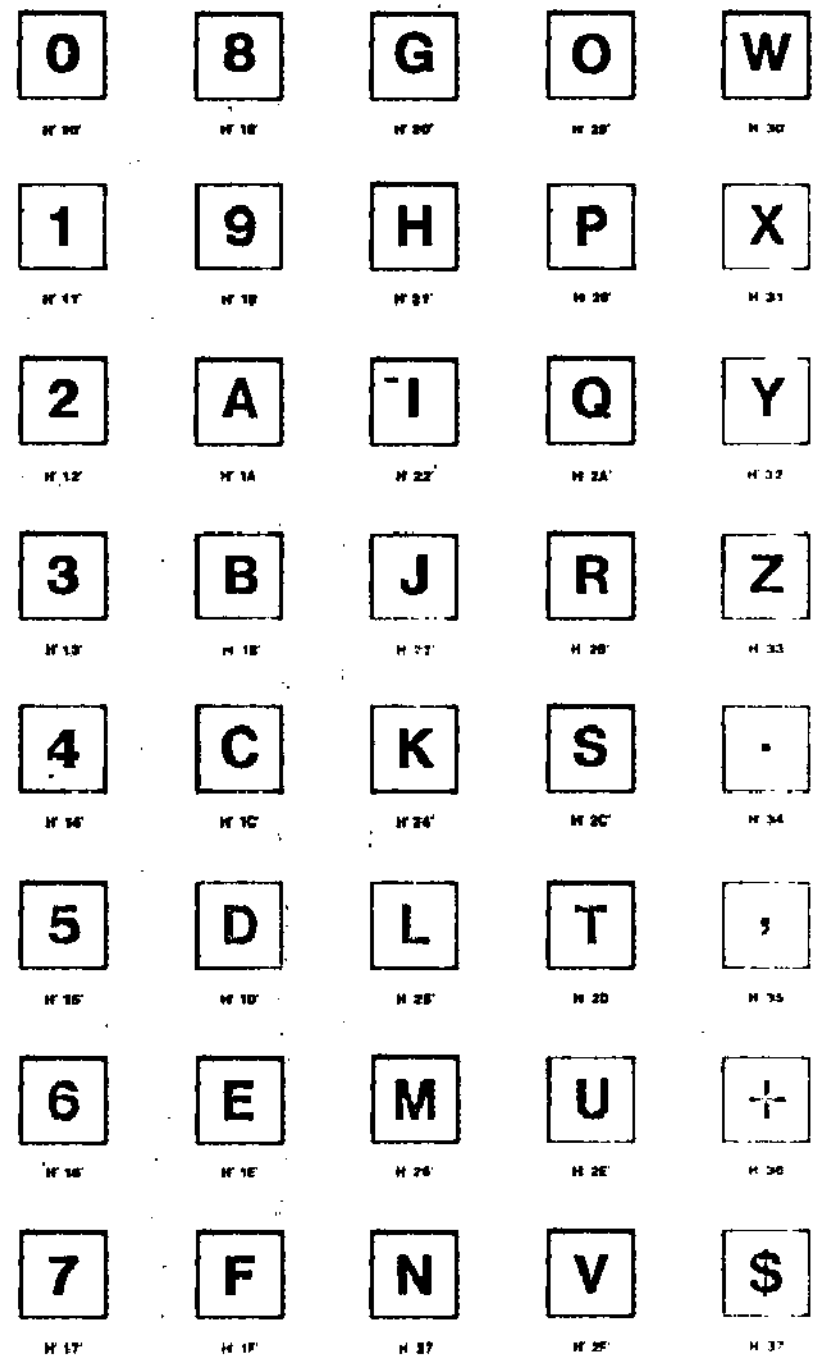


Figure 10

For different upper and lower displays, the external RAM must be dynamically refreshed if only 256 bytes of RAM are used.

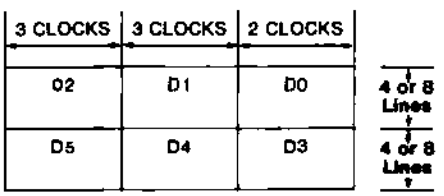
Character DMA—Refresh Mode

In the refresh mode there are 28 DMAs per frame with numbers:

15, 0, 1, 2, . . . 11, 12, 8, 1, 2, . . . 11, 12, 13

Graphics Mode

When in the graphics mode, the affected characters will be displayed in a graphics font determined by the bit pattern of the character code. D5 through D0 describe the font as follows:



Graphics Mode Control

At the beginning of each TV scan line, graphics mode is determined by the state of the GMODE bit at UVI address H'1F8':

(GM = 1) set graphics mode
(GM = 0) reset graphics mode

Additional graphics mode control is provided by two special character codes:

11000000 display blank and set graphics mode
01000000 display blank and reset graphics mode

SOUND GENERATION

Sound is generated from a pulse train of square waves at a programmed frequency. There are three types of control:

1. Fixed frequency control
2. Random noise with variable clock rate
3. Loudness control

The sound output is a combination of 1 and 2 with levels controlled by 3.

Fixed Frequency Control

The 7 bit value N (see external memory map in figure 3) is direct memory accessed to a binary counter to give frequencies such that 1/frequency = 2 (n + 1) × (horizontal line period). A value of '0' inhibits frequency generation. F_{EN} = 0 inhibits frequency output to sound channel.

Random Noise

When the random noise control (RNG) bit is set, the random number generator is reset and will start counting with a variable clock rate of N × (horizontal line period). N = the 7 bit value specified. RNG = 0 inhibits random noise to sound channel.

Loudness Control

Loudness can be controlled by LS_2 LS_1 LS_0 to give 8 levels of current output.

LS_2 LS_1 LS_0 = 000	Level 1	OFF
LS_2 LS_1 LS_0 = 001	2	
LS_2 LS_1 LS_0 = 010	3	
LS_2 LS_1 LS_0 = 011	4	
LS_2 LS_1 LS_0 = 100	5	
LS_2 LS_1 LS_0 = 101	6	
LS_2 LS_1 LS_0 = 110	7	
LS_2 LS_1 LS_1 = 111	8	LOUDEST

The levels are adjusted to be spaced equally apart.

Object Size

The least screen area occupied by each object is described by an 8 clock wide by 8 line area. Objects can be enlarged to 8 × 16. As indicated in the memory map, control bits Sz_i can be independently programmed to perform this enlargement.

Object Shape

As indicated in the memory map, the shape of an object is described by an 8-byte array. Each byte represents the video for one line of eight clocks. Figure 11 details the video output of a ball represented by the object shape array.

Object Position

Positioning the object video (and effecting motion) is accomplished by setting VC and HC in the appropriate object position. Each are 8-bit unsigned values representing the number of lines to skip (VC) and the number of clocks to skip (HC) before presenting the object video. Each has a fixed offset to VRST and HRST.

POTENTIOMETER

Four potentiometer inputs (1, 2, 3, 4) are multiplexed by control flip flop P to give two 8-bit values (see figure 6, memory map).

Data is valid during VRST; the potentiometer is set to H'FF' on the trailing edge of VRST.

OBJECT VIDEO GENERATION

Each object video generator consists of four data structures:

1. Object Size — 1-bit
2. Object Shape — 64 bits
3. Object Position — 16 bits
4. Object Color — 3 bits

HC and VC describe the position of the left-most clock and top-most line of the object video, i.e., the boxed-in bit of the ball shape.

0	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
0	1	1	0	0	0	0	0, etc.

If the HC is set to >227, the object is effectively removed from the video field.

Object Color

Object video is only displayed when bits set to 1 in the shape array are present, in which case the selected color (wire-OR with the color of any other object simultaneously being displayed) is output on pins C1, C2 and C3. When bits set to 0 are present, then the colors generated by other objects or the characters/screen are output.

As indicated in the memory map, each of the four objects is assigned a 3-bit variable (C_{ij}) which can be programmed to one of eight colors.

COLOR SYSTEM

Eight 3-bit variables are assigned to locations within the UVI memory; one for each of the four objects, two for characters, and two for screen color, i.e., character video = 0. The possible simultaneous presentation of video (object/characters) requires color precedence resolution as follows:

1. Colors of objects are wired-ORed and take precedence over characters and screen color.
2. An additional pin representing the logical OR of all object video is available to give a different color signal to differentiate between characters and objects.

STATUS REGISTERS

Three classes of status are provided:

1. Inter-object collision (6 bits)
2. Object collision with characters (4 bits)
3. ROW status - DMA number (4 bits)

The status classes 1 and 2 are presented as 2 bytes of UVI data. They should be read during vertical reset period. Status class 3 is a byte in the external RAM.

Inter-Object Collision

Six bits provide inter-object collision detection. Each is set to 0 when the AND of the appropriate two object videos is high. Each is reset to 1 when accessed or at the end of the vertical blanking period.

Object Collision with Characters

Four bits provide object-characters collision indication. Each is set when the AND of the appropriate object and background videos is high. Each is reset when accessed or at the end of the vertical blanking period.

Row Status

Four bits in the external 2112 RAM, location 255, provides information indicating the last DMA number. The status can be accessed anytime in the field when the microprocessor is not paused.

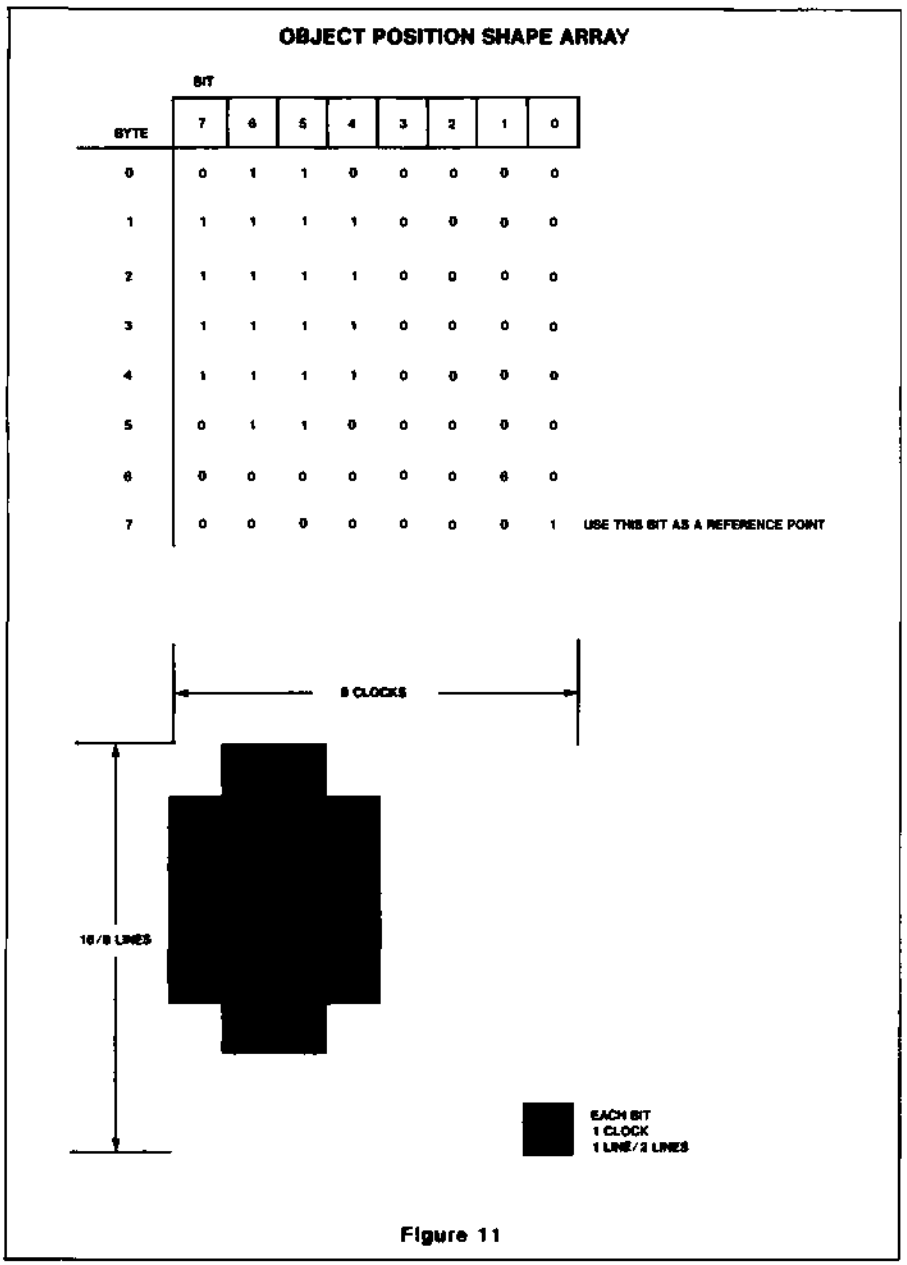


Figure 11

PRELIMINARY SPECIFICATION

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +55	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +7.0	V

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +55°C, V_{CC} = 5V ± 5%[4,5,6,7]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
I_L	Input leakage	$V_{SS} \le V_{IN} \le V_{CC}$			10	µA
I_{OL}	Output leakage (A0-A8, D0-D8) high impedance state	$V_{SS} \le V_{OUT} \le V_{CC}$			10	µA
V_{IL}	Input low voltage (all except POT1, POT2, POT3, POT4)		−0.5		0.8	V
V_{IH}	Input high voltage (all except POT1, POT2, POT3, POT4)		2.2		V_{CC}	V
V_{ITH}	Input threshold voltage for A/D (inputs POT1, POT2, POT3, POT4)			1.6		V
V_{OL}	Output low voltage (all except $\overline{OPACK}$, $\overline{C0}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, SOUND)	I_{OL} = 1.6mA			0.45	V
V_{OL1}	Output low voltage for open drain output ($\overline{OPACK}$)	I_{OL} = 2.2mA			0.45	V
V_{OL2}	Output low voltage for open drain outputs ($\overline{C0}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$)	I_{OL} = 3mA, V_{CC} = 5.25V or I_{OL} = 2.7mA, V_{CC} = 4.75V			0.45	V
V_{OH}	Output high voltage (all except $\overline{OPACK}$, $\overline{C0}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, SOUND)	I_{OH} = −100µA	2.4			V
C_{IN}	Input capacitance	V_{IN} = 0V			20	pF
C_{OUT}	Output capacitance	V_{IN} = 0V			20	pF
I_{CC}	V_{CC} Supply current	V_{CC} = 5.25V			200	mA

N. "L"

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 58°C/W junction to ambient (ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages higher than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at 50% level for inputs and at the 0.8V or 2.0V level for outputs. Input levels are 0.45V and 2.4V.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. In normal operation, the PCK, HRST and VRST inputs for the 2637 and the CLOCK input for the 2650 are obtained from the 2622 Universal Sync Generator. See 2622 data sheet for timing of these signals.

AC ELECTRICAL CHARACTERISTICS T_A = 0 to +55°C, V_{CC} = 5V ± 5%[4,5,6,7]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
t_P	PCK period[8]	NTSC and PAL	280			ns
t_{WH}	PCK high[8]	NTSC and PAL	90		150	ns
t_S	Set up time to PCK leading edge (HRST, VRST)[8]		100		280	ns
N_{TP}	Number of PCK periods per HRST period[8]	NTSC and PAL		227		
N_{TP1}	Number of HRST periods per VRST period[8]	NTSC		262		
N_{TP2}		PAL		312		
t_S	OPREQ set-up to PCK to guarantee timing[8]		100		200	ns
t_{AS}	A0-A8 and CS set-up to and hold from OPREQ[8,10]		50			ns
t_{AH}			50			ns
t_{RWS}	R/W set up to and hold from OPREQ[9,10]		50			ns
t_{RWH}			0			ns
t_{DBS}	D0-D7 set up to OPREQ and hold from PCK (P5)[9,10]	Write to UVI	50			ns
t_{DBH}			0			ns
t_{CAKL}	PCK (P4) to $\overline{OPACK}$ low delay and	R_L = 5K, C_L = 100pF or			400	ns
t_{CAKH}	PCK (P5) to $\overline{OPACK}$ high delay[9,10]	R_L = 10K, 1 TTL, C_L = 50pF			1.0	µs
t_{DA}	D0-D7, PCK (P3) to data bus valid[9,10]	Read of UVI; C_L = 100pF, 1 TTL or C_L = 100 pF			400	ns
t_{DV}	D0-D7: Data bus valid[9,10]	Read of UVI; C_L = 100pF, 1 TTL or C_L = 100pF	3.0			µs
t_{CRTS}	D0-D7: OPREQ low to data bus 3-state delay[9]	Read of UVI			200	ns
t_{PSL}	PCK (40) to $\overline{PAUSE}$ low and	C_L = 53pF and 1 TTL load			400	ns
t_{PSH}	PCK (221) to $\overline{PAUSE}$ high[11]					
t_{AEH}	PCK (4) to $\overline{ADEN}$ high and	C_L = 50pF and 1 TTL load			400	ns
t_{AEL}	PCK (221) to $\overline{ADEN}$ low[11]					
t_{AD}	PCK to AD to A8 valid[12,13]	C_L = 100pF and 1 TTL load or C_L = 100pF			400	ns
t_{RCEL}	PCK to $\overline{RCE}$ low and high[12,13]	C_L = 50pF and 1 TTL load			400	ns
t_{RCEH}					400	ns
t_{RWL}	PCK to R/$\overline{W}$ low and high[12,13]	C_L = 50pF and 1 TTL load; DMA write			400	ns
t_{RWH}					400	ns
t_{DS}	D0-D7 set up to PCK loading edge[12,13]	DMA RAM read	100			ns
	Allowable external RAM access time:[12,13]					
t_A	From address valid	DMA RAM read			1.2	µs
t_{CO}	$\overline{RCE}$ low				1.0	µs

NOTES
For 4,5,6,7, see previous page.
8. See figure 12
9. See figure 13
10. See figure 14.
11. See figure 15.
12. See figure 16.
13. See figure 17.
14. See figure 18

AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
t_{DA}	Data bus delay: PCK (40) to data valid[2]	C_L = 100pF and 1 TTL load or C_L = 100pF DMA RAM write			400	ns
t_{DH}	Data bus hold: Data valid after PCK (45)[2]	C_L = 100pF and 1 TTL load or C_L = 100pF DMA RAM write	280			ns
t_{AKL} t_{AKH}	OPREQ to $\overline{OPACK}$ low and high[4]	R_L = 5K/V_{CC}, C_L = 50pF or R_L = 10K/V_{CC}, C_L = 50pF and 1 TTL load			250 1.0	ns µs
t_{CEON} t_{CEOFF}	OPREQ to $\overline{CE}$ low and high[4]	C_L = 50pF and 1 TTL load			250 250	ns ns
t_S	OPREQ set up to PCK[5]		100			ns
t_{AS} t_{AH}	Set up to and hold from OPREQ A0-A8 and CS[5]		50 50			ns ns
t_{DBS} t_{DH}	Set up to and hold from OPREQ D0-D7[5]		50 50			ns ns
t_{RWS} t_{RWH}	Set up to and hold from OPREQ $\overline{R}/W$[5]	Write to ext RAM	50 50			ns ns
t_{CAKL} t_{CAKH}	PCK (P4) to $\overline{OPACK}$ low delay and PCK (P6) to $\overline{OPACK}$ high delay[5]	R_L = 5K, C_L = 100pF or R_L = 10K, 1 TTL load, C_L = 50pF			400 1.0	ns µs
t_{RWL} t_{RWH}	PCK (P1) to R/$\overline{W}$ low and PCK (P7) to R/$\overline{W}$ high[5]	C_L = 50pF and 1 TTL load RAM write			400 400	ns ns
t_{RCEL} t_{RCEH} t_{RCEW}	PCK (P2) to $\overline{RCE}$ low[5] PCK (P5) to $\overline{RCE}$ high $\overline{RCE}$ low duration	C_L = 50pf and 1 TTL load RAM write		 700	400 400 	ns ns ns
t_{RCELR} t_{RCEHR}	OPREQ to $\overline{RCE}$ low and high[5]	C_L = 50pF and 1 TTL load RAM read			400 400	ns ns
t_{VL} t_{VH}	PCK to video low and high[6]	R_L = 1.8K/V_{CC}, C_L = 50pF			200 200	ns ns

The SOUND frequency is generated internally by a seven bit binary counter and a nine bit pseudo random counter. The binary counter downcounts a value to zero, toggles a flip-flop, clocks the random counter and reloads the value. Any combination of the two frequencies can be logically switched to the SOUND pin under software control.

There are three parallel, open drain output buffers on the SOUND pin. Each buffer has a different geometry and is enabled by a separate control bit. Thus, if the pin is biased at constant voltage, holding the output buffers in the saturated region, the SOUND output will act as a variable current source. Eight relative values of current are possible depending upon the codes in the three control bits. The resultant current will be a summation of the currents of each enabled buffer, each of which are proportional to the respective buffer geometries.

ENABLE CODE LS_2	LS_1	LS_0	TEST CONDITIONS	I_{OUT} Min	I_{OUT} Typ	I_{OUT} Max	UNITS
0	0	0	V_{OUT} = 2.0V			10	µA
0	0	1			I_O[7]		µA
0	1	0			$2I_O$		µA
0	1	1			$3I_O$		µA
1	0	0			$4I_O$		µA
1	0	1			$5I_O$		µA
1	1	0			$6I_O$		µA
1	1	1			$7I_O$		µA

NOTES

1. See figure 15
2. See figure 16
3. See figure 17
4. See figure 18
5. See figure 19
6. See figure 20
7. I_O = 300 µA typically

TIMING DIAGRAMS

CLOCK AND INPUT TIMING

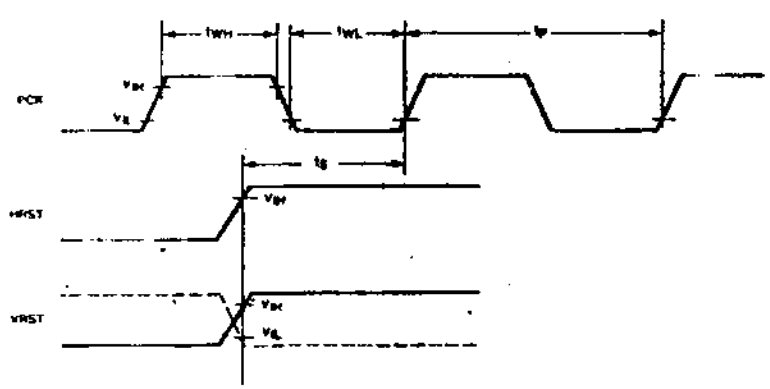


Figure 12

UVI READ/WRITE TIMING

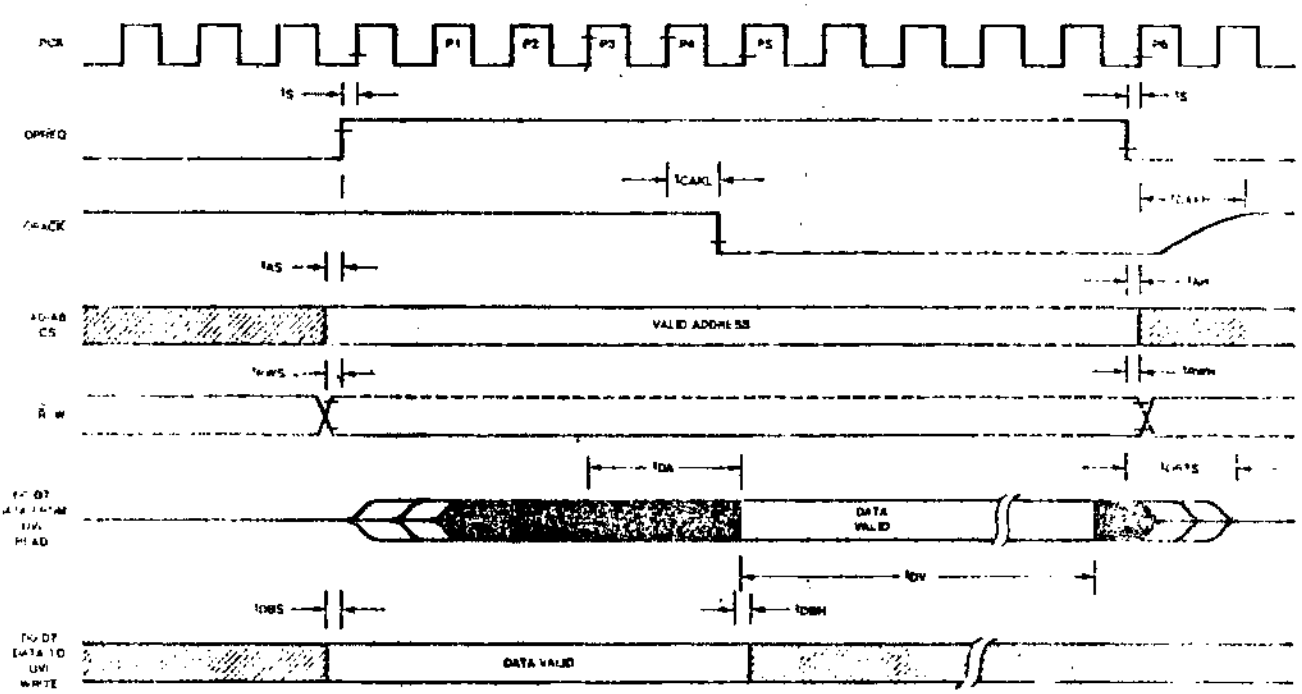


Figure 13

PRELIMINARY SPECIFICATION

TIMING DIAGRAMS (con't)

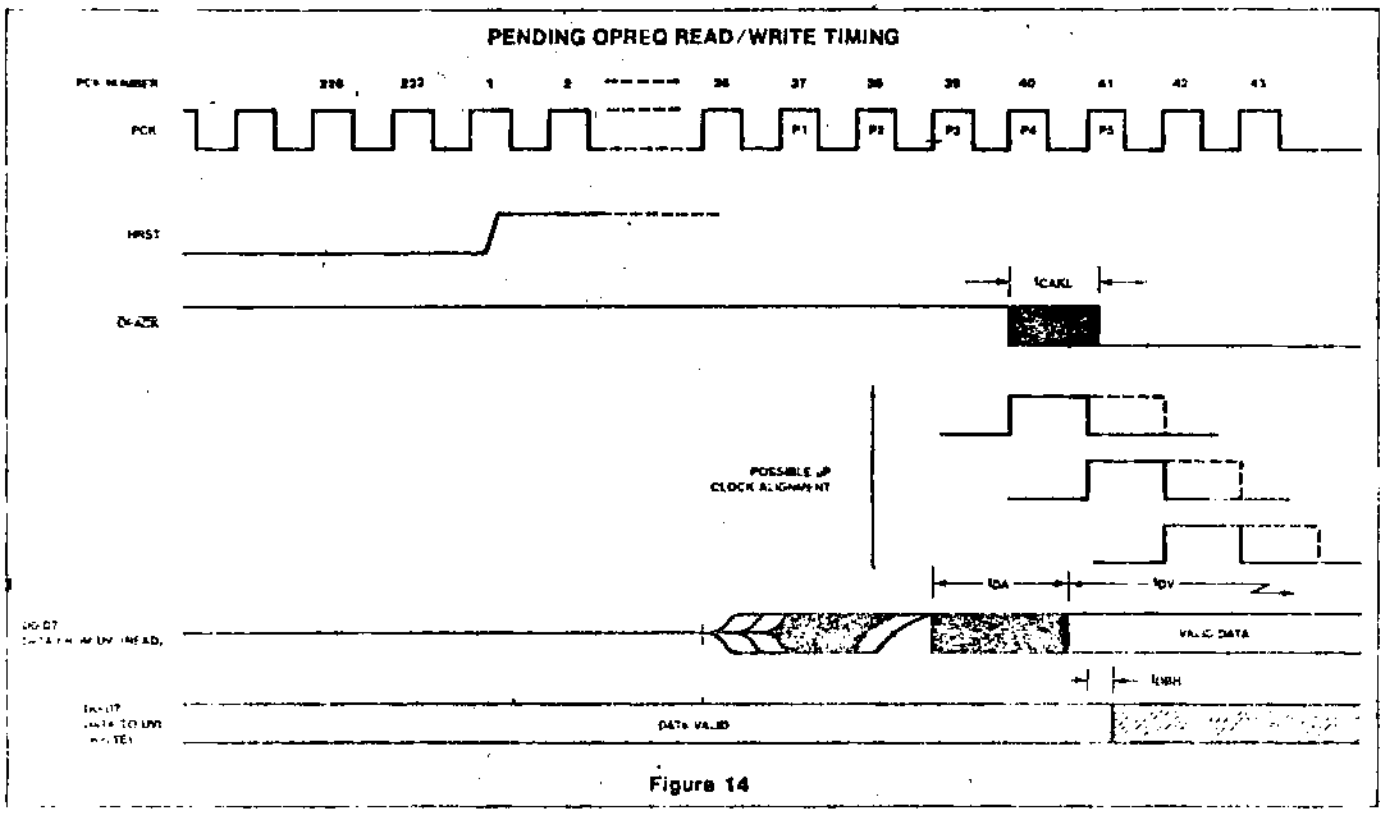


Figure 14

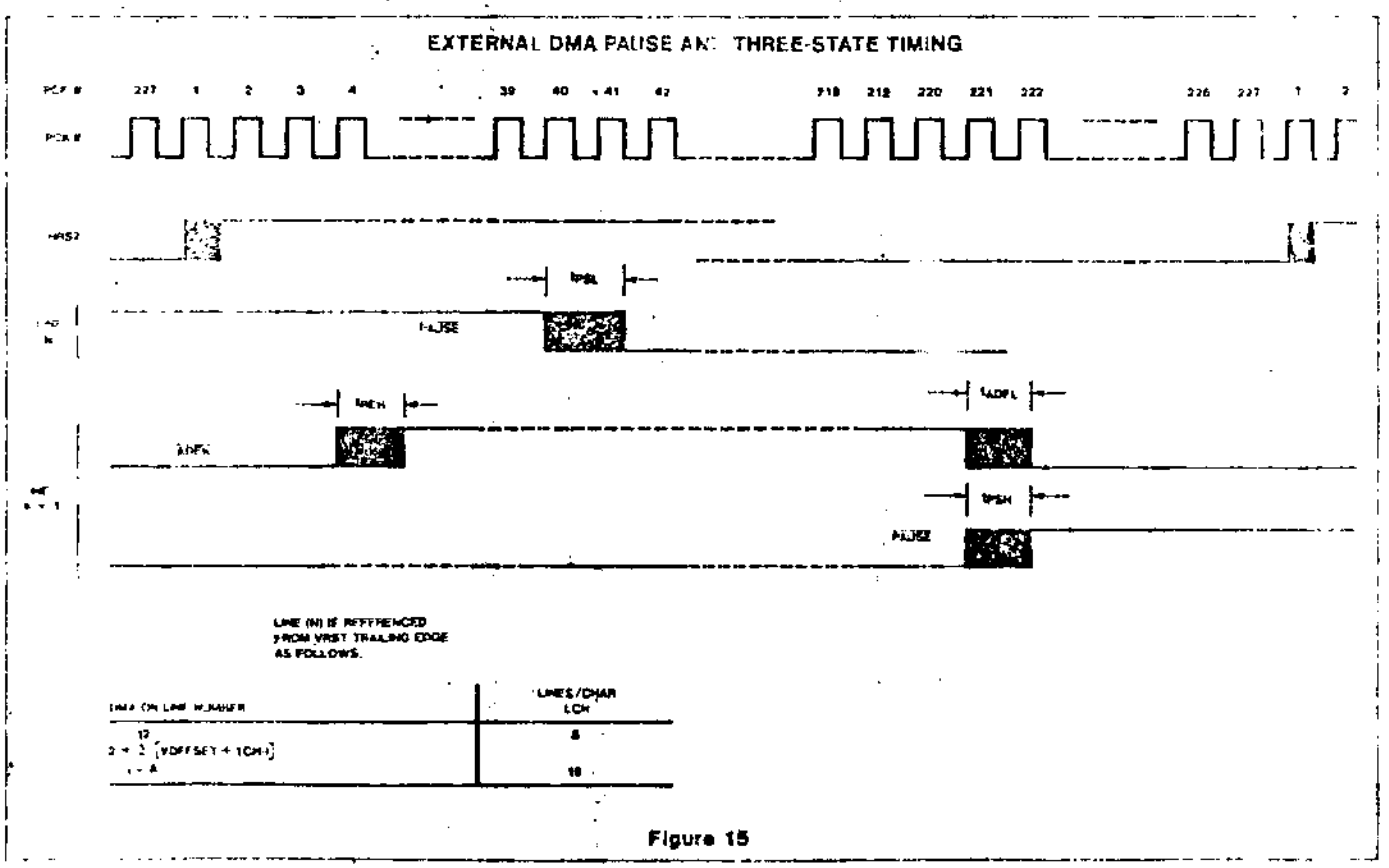


Figure 15

TIMING DIAGRAMS (con't)

UVI EXTERNAL DMA TIMING BEGINNING OF LINE

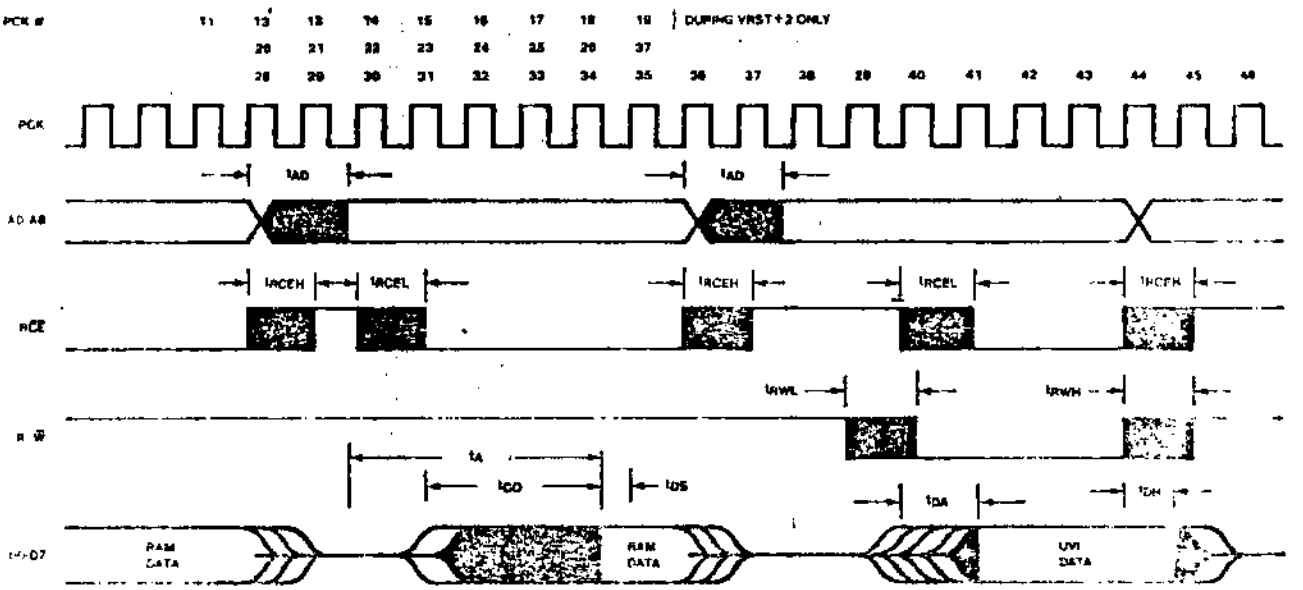
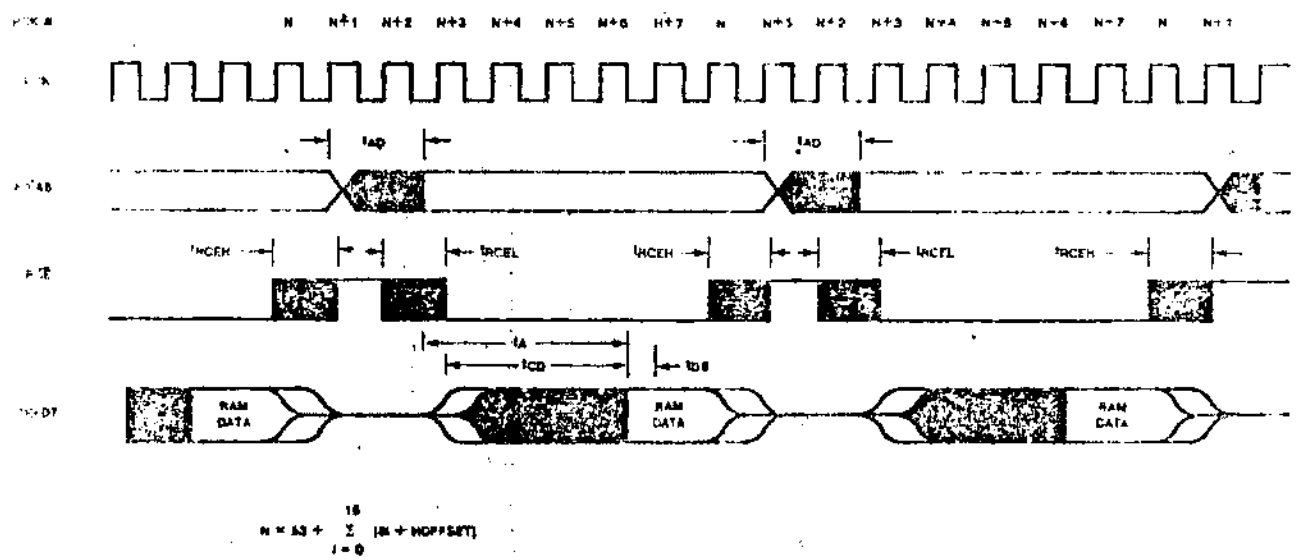


Figure 16

UVI EXTERNAL DMA TIMING MIDDLE OF LINE CHARACTER FETCH

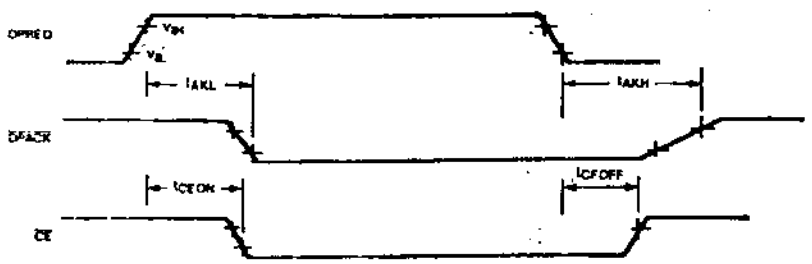


$$N = \Delta 3 + \sum_{I=0}^{15} (M + HOFFSET)$$

Figure 17

TIMING DIAGRAMS (con't)

UNCLOCKED ACCESS MODE OPACK AND CE TIMING



NOTE
Above OPACK timing is held for all accesses to the CE field and for all accesses with the CS input at a logic ZERO

Figure 18

READ/WRITE μP RAM ACCESS TIMING THRU UVI R/$\overline{W}$ AND RCE INPUTS

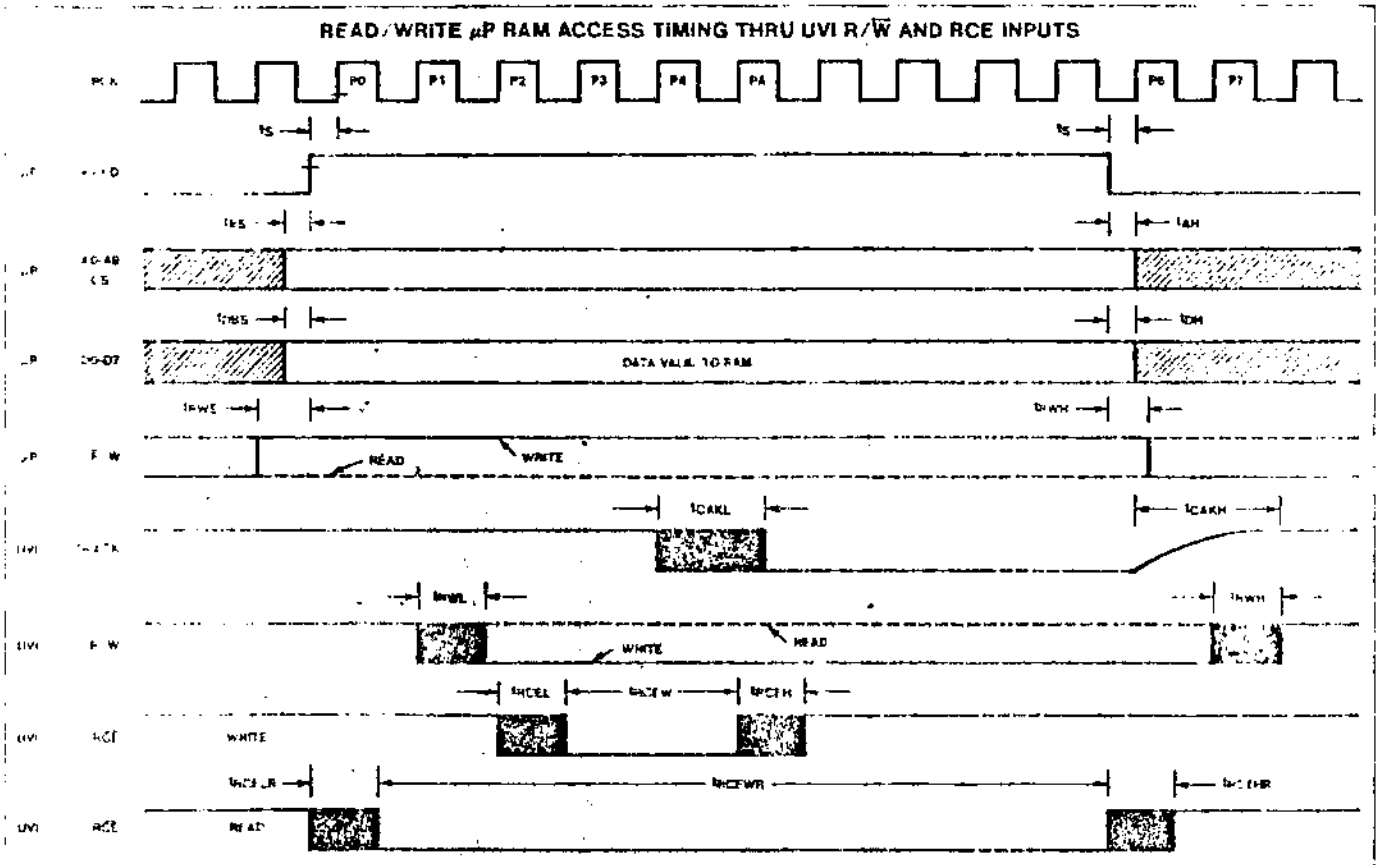


Figure 19

VIDEO OUTPUT TIMING

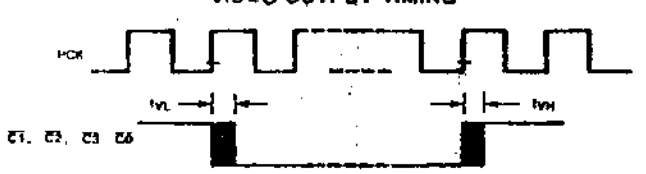


Figure 20