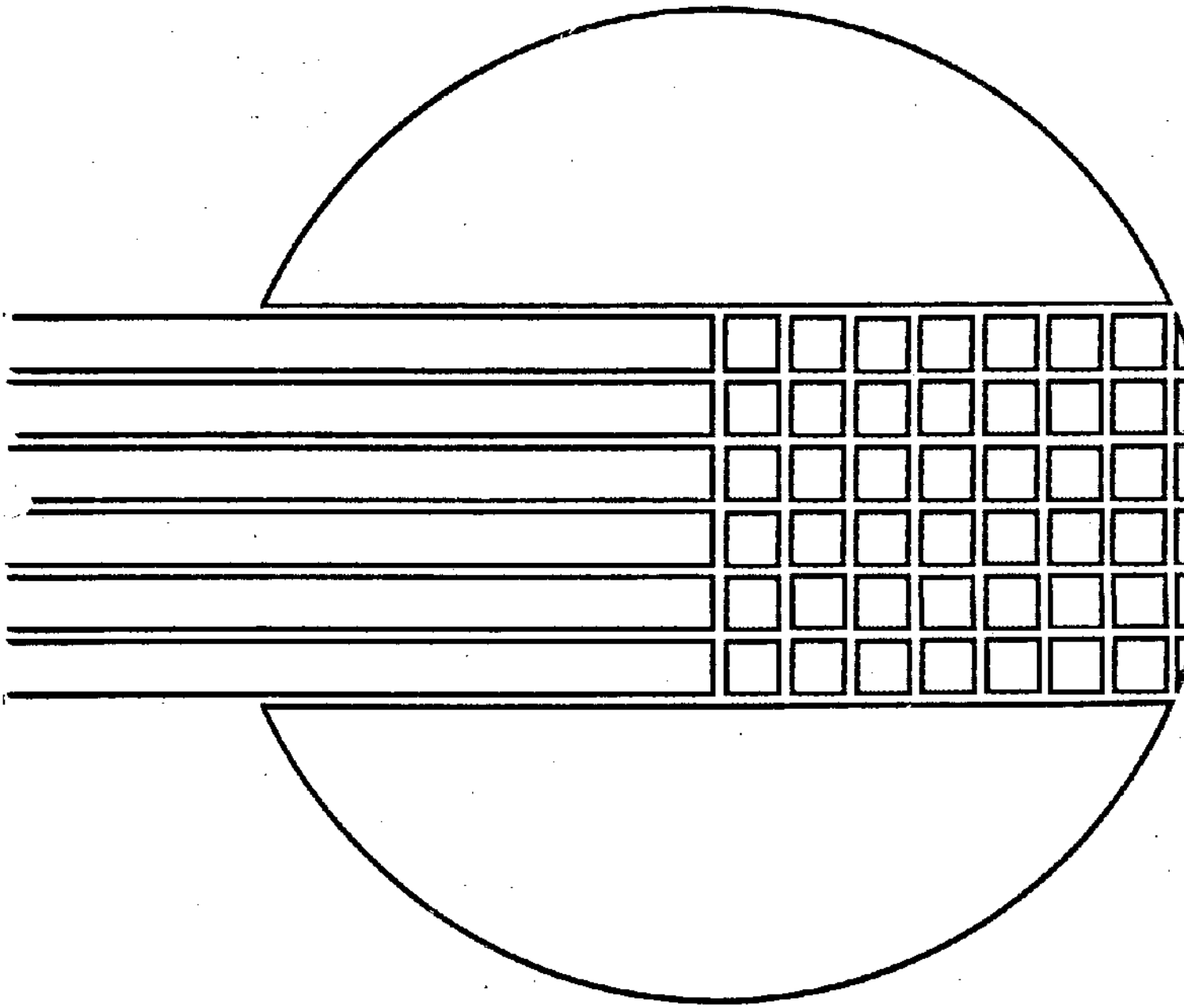
SIGNETICS PROGRAMMABLE VIDEO INTERFACE (PVI) 2636



VALVO

PROGRAMMABLE VIDEO INTERFACE (PVI) 2636

PRELIMINARY SPECIFICATION 2636I

DESCRIPTION

The Signetics 2636 Programmable Video Interface (PVI) is intended for use in microprocessor-controlled game systems, and provides all of the common game circuits on a single chip. Circuits are provided for player inputs, background, moving objects, scoring, and audio signals.

A typical system configuration consists of five LSI circuits: a PVI, a 2616 16K ROM, an NE549 Digital Video Summer (DVS) a Universal Sync Generator (USG), and a 2650A microprocessor.

Additional PVIs as well as random logic can easily be interfaced to enhance game complexity. Since the system is microprocessor based, the actual game itself need not be "hardwired" into the system. Game definition is completely contained in the ROM. To change games, one simply replaces one ROM with another. Each ROM can contain several games, depending on game complexity and similarity between games.

The 2636 PVI, is constructed using Signetics' silicon gate N-Channel depletion load technology and operates from a single +5 volt power supply.

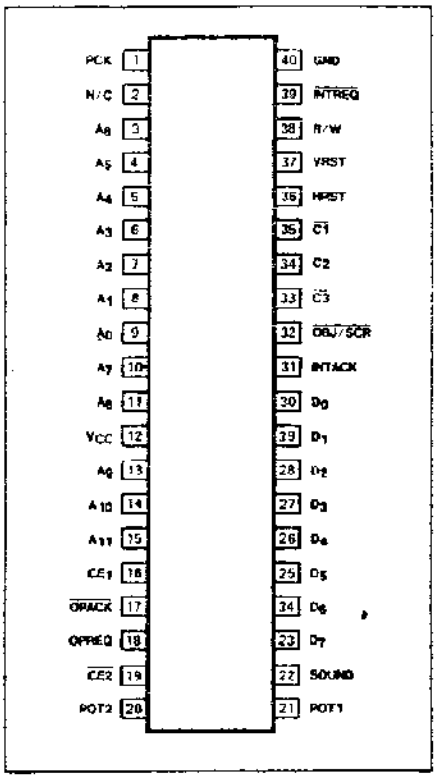
FEATURES

- Four general-purpose, RAM-resident object modules
- Object duplication permitting generation of up to 80 object images on the screen
- 280ns object resolution
- Object size and position under program control
- Programmable score
- Programmable sound
- Programmable background
- Eight programmable colors with multiple brightness levels
- 37-byte scratch pad memory
- Chip Enable outputs for system ROMs and PROMs
- I/O facilities for switch scanning and potentiometer inputs
- Wire-OR expansion capability to multiple PVIs
- Forty-pin dual-in-line package

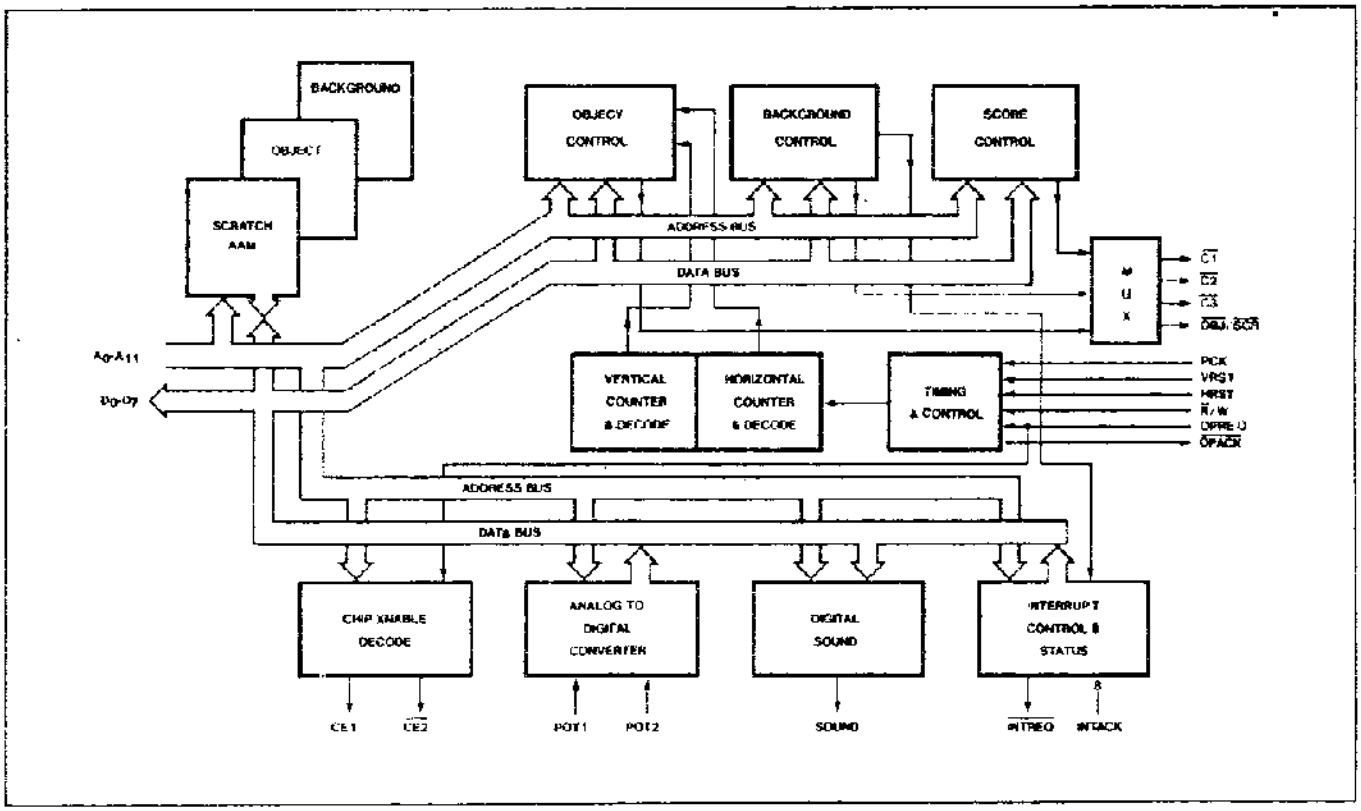
APPLICATIONS

- Consumer programmable video games
- Arcade games
- Simulators
- Special purpose graphic displays
- Home computer center

PIN CONFIGURATION



PVI BLOCK DIAGRAM

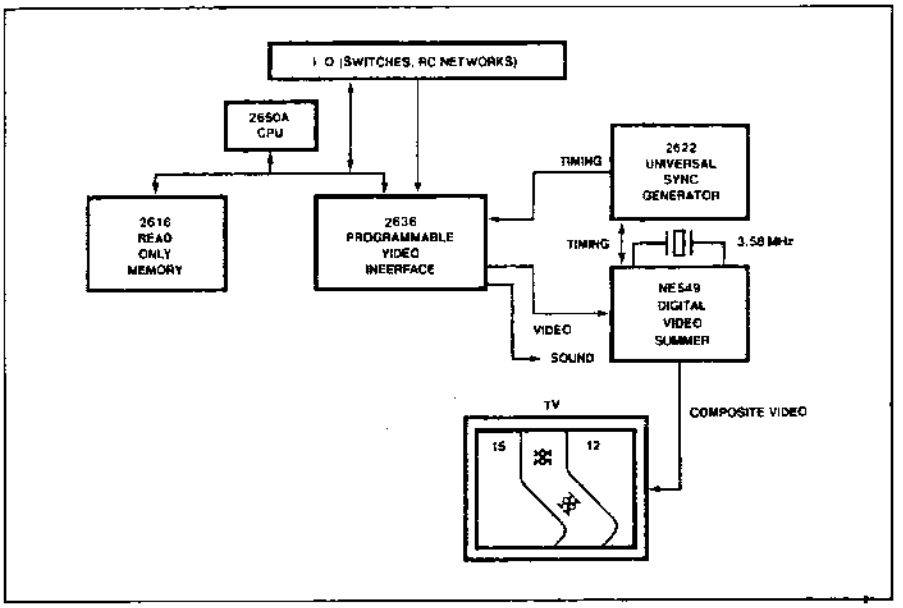


SYSTEM OVERVIEW

A block diagram of a typical TV game system is shown below. The Signetics 2650A microprocessor reads the game program stored in ROM and controls the video presented to the TV. The PVI serves as a programmable video generator, interpreting microprocessor commands and presenting video to the DVS. The DVS accepts digital video signals from the PVI and timing signals from the USG and generates composite video for a TV monitor.

The 2650A communicates with the PVI over the address bus and data bus. The PVI looks like part of the memory field to the microprocessor. The 2650A writes data into the PVI's RAM field. The PVI in turn generates video that reflects the information stored in its RAM. The PVI also presents the 2650A with I/O and status information (e.g., object collisions) by writing that data in its RAM field. The microprocessor can then read the I/O data and make decisions accordingly.

SYSTEM BLOCK DIAGRAM



PVI FUNCTIONAL DESCRIPTION

The 2636 PVI is a bus-oriented device. The 2650A address and data buses enter the PVI and access the major functional blocks. With the address bus the microprocessor selects which block it wishes to communicate with. The information is presented to or received from the selected block on the data bus.

The 2622 USG provides the basic clock frequency and the horizontal and vertical reset signals to the PVI. These signals drive the vertical and horizontal counters. The counters provide the PVI with a Cartesian coordinate representation of the television screen (i.e., each counter pair describes a unique point on the screen.)

The OBJECT and BACKGND memory stores the video patterns digitally. Both the 2650A

PIN DESIGNATION

MNEMONIC	TYPE	NAME & FUNCTION
A0-A11	I	**Address Bus:** 12-bit address bus.
D0-D7	I/O	**Data Bus:** 12-bit data bus.
OPREQ	I	**Operation Request:** When this signal is high, all signals from the 2650A are valid.
R/$\overline{W}$	I	**Read/Write:** Specifies the direction of data transfer. Read when low, write when high.
$\overline{OPACK}$	O	*__Operation Acknowledge:__ The PVI pulls this signal to ground when it is ready to service the 2650A.
$\overline{INTREQ}$	O	*__Interrupt Request:__ The PVI requests service from the microprocessor by pulling this output low.
INTACK	I	**Interrupt Acknowledge:** This signal is returned to the PVI when the microprocessor has accepted an interrupt request.
PCK	I	**Position Clock:** Generated by the 2622 USG to synchronize the PVI's internal functions. (3.58MHz, 227 pulses/line).
$\overline{C1}$,$\overline{C2}$,$\overline{C3}$	O	*__Color 1, Color 2, Color 3:__ Outputs denoting the color to be displayed.
VRST	I	**Vertical Reset:** The 2622 USG provides this signal to synchronize the PVI's vertical counter.
HRST	I	**Horizontal Reset:** This signal is provided by the 2622 USG to synchronize the PVI's horizontal count chain.
CE1	O	**Chip Enable One:** This output is high when the address bus value is in the range H'000' to H'0FF'. May be used to enable the ROM.
POT1, POT2	I	**Potentiometer 1,2:** These pins connect to external variable RC networks for A/D conversion.
$\overline{CE2}$	O	**Chip Enable Two:** This pin is low when the address bus is in the range H'E60' to H'EFF'.
SOUND	O	**Digital Sound:** An audio frequency square wave output generated under program control.
$\overline{OBJ/SCR}$	O	*__Object/Score:__ This output goes low when the PVI is presenting either object or score video information. It serves as the fourth color output. It can also be used, with additional logic, to detect object collisions in multiple PVI systems.
V_{CC}	I	**Power Supply:** +5V ±5%
GND	I	**Ground:** 0V reference ground.

Note

*Indicates open-drain outputs

and the PVI have access to this information. PVI control circuits look at the information stored in the memory by the microprocessor (e.g., place object one at H-120, V-37) and generate the specified video at the proper location. The outputs are the colors of the objects, background and score, and a tone frequency.

The A/D Block converts the analog potentiometer position information into binary data for the microprocessor.

The Digital Sound block is a square wave generator whose output frequency is controlled by the microprocessor.

The Interrupt Control and Status block allows the PVI to request service from the 2650A and provides status information to the microprocessor.

2650A INTERFACE AND ADDRESS SPACE

The 2650A communicates with the PVI exclusively through memory addressing. Each PVI has control over 4K of address space, as shown in Figure 1. Two hundred and fifty-six addresses H'F00' to H'FFF' are used internally in the PVI as object and background description, scratchpad, and control. Addressing the first 3½K will activate CE1—an active high output enable signal for external ROM. $\overline{CE2}$ is active low when H'E80' to H'EFF' are addressed.

$\overline{OPACK}$ coming out of the PVI is externally pulled to the '1' state. When the PVI is accessed, $\overline{OPACK}$ will go low when the PVI has the data ready on the bus. When addresses outside the range H'F00' to H'FFF' are accessed, $\overline{OPACK}$ will be pulled low shortly after the leading edge of OPREQ.

The PVI generates an interrupt request signal at the leading edge of each vertical reset and on completion of the video generation of an object. In the latter case, the interrupt is generated at the last line of that object video. The interrupt address H'0003' is generated when the interrupt request is acknowledged. Interrupts are reset on the trailing edge of the vertical reset signal.

INTERNAL MEMORY ORGANIZATION

The PVI contains data structures which:

a) Describe the shape, color and size of four objects and duplicates of those objects.

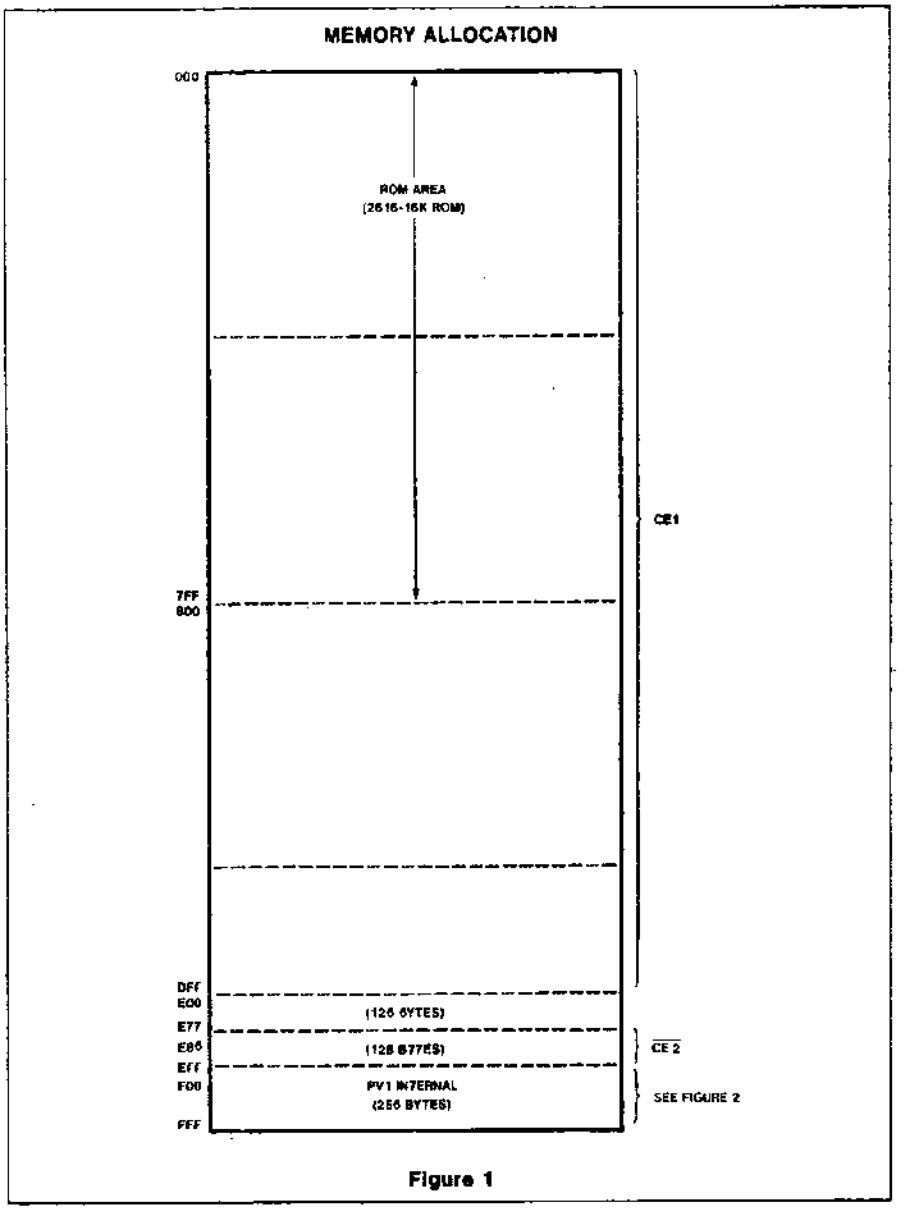


Figure 1

b) Describe the shape and color of the background.

c) Retain sound and score data.

d) Describe inter-object and object-background collision, object video display completion, and field completion.

e) Retain the latest A/D conversion of potentiometer inputs.

f) Provide scratch RAM area for program computations.

Figure 2 is the internal memory map of the PVI showing the location of the various data structures.

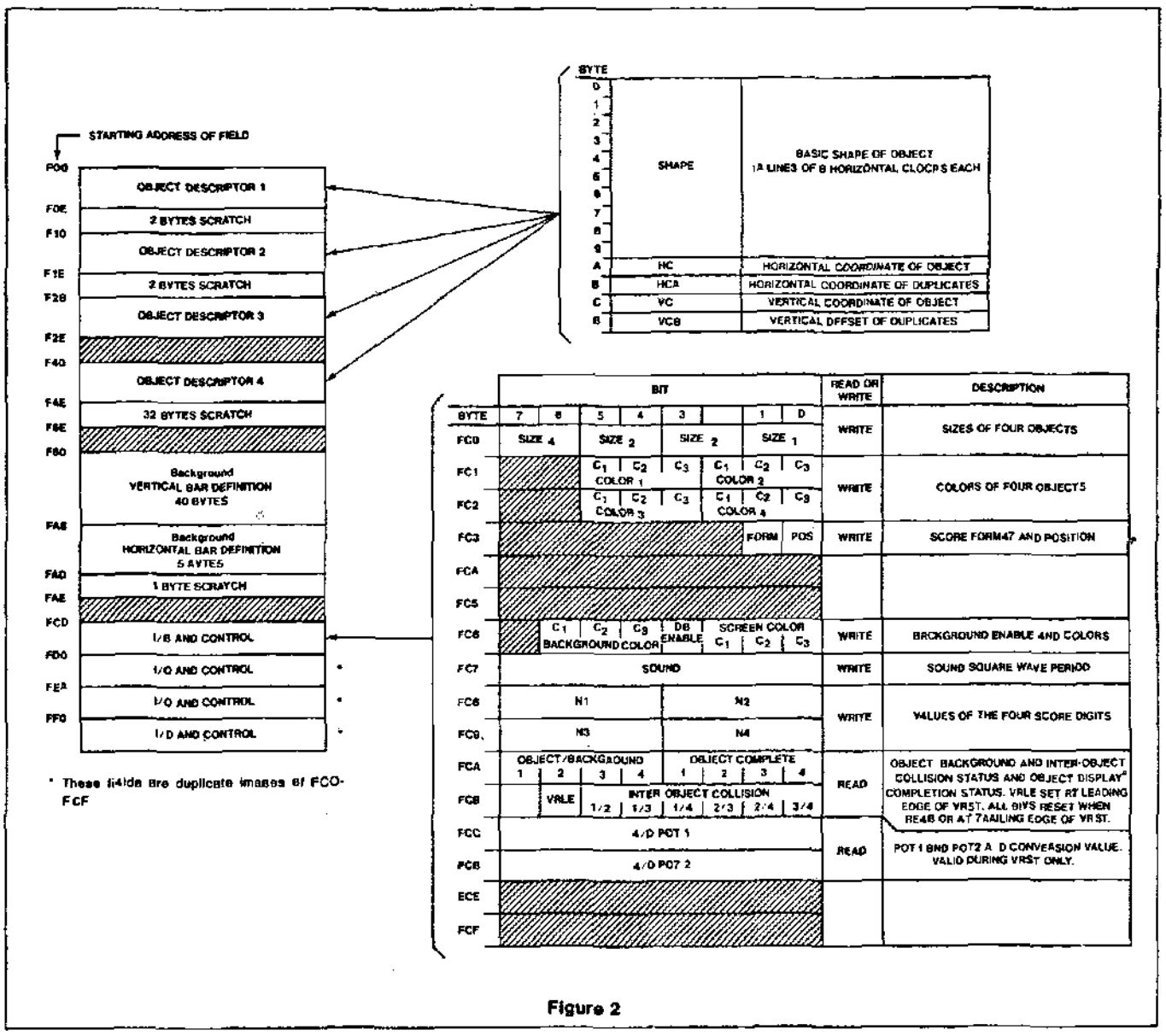

STARTING ADDRESS OF FIELD
F00
OBJECT DESCRIPTOR 1
F0E
2 BYTES SCRATCH
F10
OBJECT DESCRIPTOR 2
F1E
2 BYTES SCRATCH
F20
OBJECT DESCRIPTOR 3
F2E
F40
OBJECT DESCRIPTOR 4
F4E
32 BYTES SCRATCH
F6E
F80
Background VERTICAL BAR DEFINITION 40 BYTES
FA8
Background HORIZONTAL BAR DEFINITION 5 BYTES
FAD
1 BYTE SCRATCH
FAE
FCD
I/O AND CONTROL
FD0
I/O AND CONTROL *
FE8
I/O AND CONTROL *
FF0
I/O AND CONTROL *
* These fields are duplicate images of FC0-FCF
BYTE
SHAPE
BASIC SHAPE OF OBJECT 16 LINES OF 8 HORIZONTAL CLOCKS EACH
HC
HORIZONTAL COORDINATE OF OBJECT
HCA
HORIZONTAL COORDINATE OF DUPLICATES
VC
VERTICAL COORDINATE OF OBJECT
VCA
VERTICAL OFFSET OF DUPLICATES
BIT
READ OR WRITE
DESCRIPTION
FC0 SIZE 4 SIZE 3 SIZE 2 SIZE 1 WRITE SIZES OF FOUR OBJECTS
FC1 FC2 COLOR 1 COLOR 2 COLOR 3 COLOR 4 WRITE COLORS OF FOUR OBJECTS
FC3 FORM POS WRITE SCORE FORMAT AND POSITION
FCA FCB
FC6 BACKGROUND COLOR DB ENABLE SCREEN COLOR WRITE BACKGROUND ENABLE AND COLORS
FC7 SOUND WRITE SOUND SQUARE WAVE PERIOD
FC8 N1 N2 WRITE VALUES OF THE FOUR SCORE DIGITS
FC9 N3 N4
FCA OBJECT/BACKGROUND OBJECT COMPLETE READ OBJECT BACKGROUND AND INTER-OBJECT COLLISION STATUS AND OBJECT DISPLAY COMPLETION STATUS. VRLE SET AT LEADING EDGE OF VRST. ALL BITS RESET WHEN READ OR AT TRAILING EDGE OF VRST.
FCB VRLE INTER OBJECT COLLISION 1/2 1/3 1/4 2/3 2/4 3/4
FCC 4/D POT 1 READ POT 1 AND POT 2 A D CONVERSION VALUE. VALID DURING VRST ONLY.
FCB 4/D POT 2
ECE
FCF

Figure 2

OBJECT VIDEO GENERATION

As shown in Figure 2, each object is described by five data structures:

- Object Size - 2 bits
- Object Shape - 80 bits
- Object Position - 16 bits
- Duplicate Object Position - 16 bits
- Object Color - 3 bits

Object Size

The least screen area occupied by each object is an 8 clock wide by 10 line high area. Each object can be individually enlarged to 16 by 20, 32 by 40, or 64 by 80 by programming four 2-bit variables named $SIZE_n$.

Figure 3 details the relative screen area for each of the four object sizes.

Object Shape

The shape of an object is described by the 10-byte array named SHAPE. Give a SIZE of 00, each byte represents the video for one line of eight clocks. The most significant bit of byte 0 corresponds to the upper left corner of the object and the least significant bit of byte 9 corresponds to the lower right corner of the object. Bits set to zero indicate no video while bits set to one cause video to be displayed with the specified object color.

Object Position

Positioning the object video (and effecting motion) is accomplished by setting VC and HC in the appropriate Object Descriptor record. Each are 8-bit unsigned values representing the number of lines to skip (VC) and the number of clocks to skip (HC) before presenting the object video. For reference, the location of the upper left corner of the background is 32H, 20V. The clocks and lines to skip to position an object at this location are therefore 31 and 19, respectively.

If HC or VC is set to >227 or >252, respectively, the object is effectively removed from the video field.

Changes to the values of HC and VC operate as follows. If HC is changed during the time that the corresponding object video is being displayed, the portion of the object not yet displayed will be displaced to the new horizontal position. The value of VC is 'remembered' at the trailing edge of VRST. Thus, if VC is changed during the active scan, the vertical object position change will not be effective until the next active scan.

Duplicate Object Position

One or more duplicates of an object may be displayed by setting HCB to the required horizontal clock position and VCB to "the number of lines—1" to skip after displaying the last line of the object video. In the case of N = 0, VCB is set to 255.

Figure 4 details two objects with duplicates each of SIZE = 00. Object 1 begins at 42, 36 and has duplicates beginning at 30H and 11 lines (skipping 10 with VCB1=9) below each previous last line. The duplicates continue until VRST is true. Object 2 begins at B2,20 and has duplicates beginning at B8H and 29 lines (skipping 28 with VCB2=27) below each previous last line.

Note that the duplicate of an object cannot overlap vertically with its primary image.

Unlike HC and VC, HCB and VCB may be changed during the scan and such changes will be effected on the current scan. HCB is sampled during each HRST. Thus, if HCB is changed during the display of a duplicate, a portion of the object will be displaced horizontally. For proper operation, HCB should be changed only after the 'Object Video Completion' status bit indicates completion of the object. VCB is sampled just prior to displaying the last line of the object. To affect a change in the vertical offset to the next duplicate, VCB must be changed before the 'Object Video Completion' status bit indicates completion of the object.

Object Color

Object video is only displayed when bits set to 1 in the SHAPE array are present, in which case the selected color (wire-OR with the color of any other object simultaneously being displayed) is output on pins $\overline{C1}$, $\overline{C2}$ and $\overline{C3}$. When bits set to 0 are present, then the colors generated by other objects or the background/screen are output.

As indicated in Figure 2, four 3-bit variables named COLOR can be programmed to provide one of eight colors for the object. The $\overline{OBJ/SCR}$ output is also activated whenever object video is displayed and can serve as a fourth color select output.

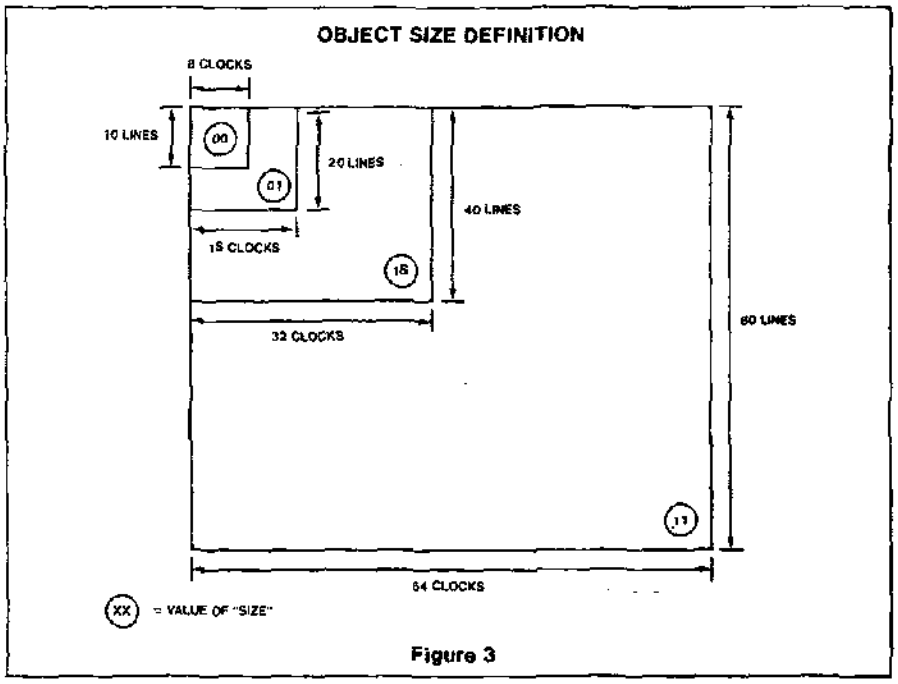


Figure 3

Object Video Completion

Four status bits indicate the completion of display of the video of each of the four objects. The signal is available at the last line of video output. This action occurs for both primary and duplicate images of an object.

Object video completion also causes an interrupt to be generated. See 2650 INTERFACE section of this data sheet.

Object Collision with Background

Four status bits provide object-background collision indication. Each is set when the AND of the appropriate object and background videos is high. Each is reset when the status byte is accessed or when VRST goes low. When duplicates of objects are being generated, the game program must determine which duplicate is responsible.

Inter-Object Collision

Six status bits provide inter-object collision detection. Each is set when the AND of the appropriate two object videos is high. Each is reset when the status byte is accessed or when VRST goes low. When duplicates of objects are involved, the game program must determine which duplicate is responsible.

DUPLICATION OF OBJECTS

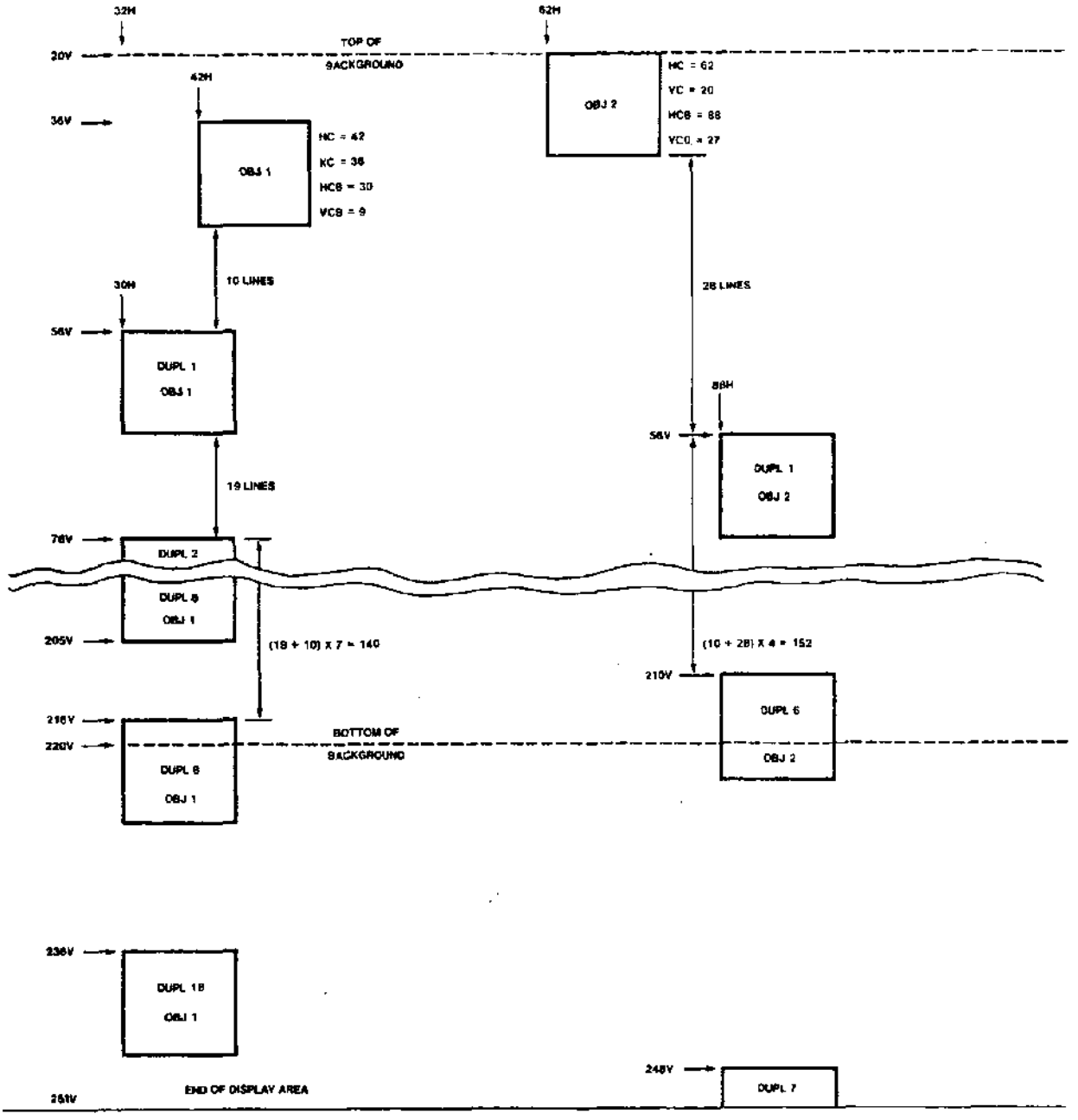


Figure 4

BACKGROUND VIDEO GENERATION

Background video generation is described through five dsta structurea:

- Vertical Bar Definition - 320 bits
- Horizontsl Bar Definition - 40 bits
- Background Enable - 1 bit
- Background Color - two groups of 3 bits each

Vertical Bar Definition

Up to 320 distinct vertical bars may be displayed. The bars are arranged in 20 vertical sets of 18 bars each (see Figvre 5). The bars of each set are 1 clock wide and horizontally separated by sevan clock positions. The first set of bars of each pair of sets is two lines on the vertical and the next set is 18 lines on the vertical, and so forth.

A 40-byte array located at F80-FA7 defines which bars are displsyed. The array is arranged in 20 sets of 16 bits. The first two bytes map the first set of 16 bars. The next two bytes map the second set of 16 bsrs, etc.

Figure 6a shows an example of vertical bar definition for the top four sets of bars on the screen.

Horizontal Bar Definition

As can be seen in the previous example, no horizontal bars exist as yet. Horizontal bars are effected by horizontally extending vertical bars. The 40 bytes of vertical bar definition describe bars 1 clock wide. Five additionel bytes are svsilable to extend vertical bars to a width of 2, 4 or 6 clocks. Each byte affects four of the previously defined sets of vertical bars as follows:

FA8 maps onto sets 1-4
FA9 maps onto sets 5-8
FAA maps onto sets 9-12
FAB maps onto sets 13-16
FAC maps onto sets 17-20

Bits 7 and 6 define all selected bars of the corresponding sets being 1, 2, or 4 clocks wide as follows:

B7	B6	Clocks/Bar
0	0	1
0	1	2
1	0	1
1	1	4

PVI BACKGROUND DEFINITION

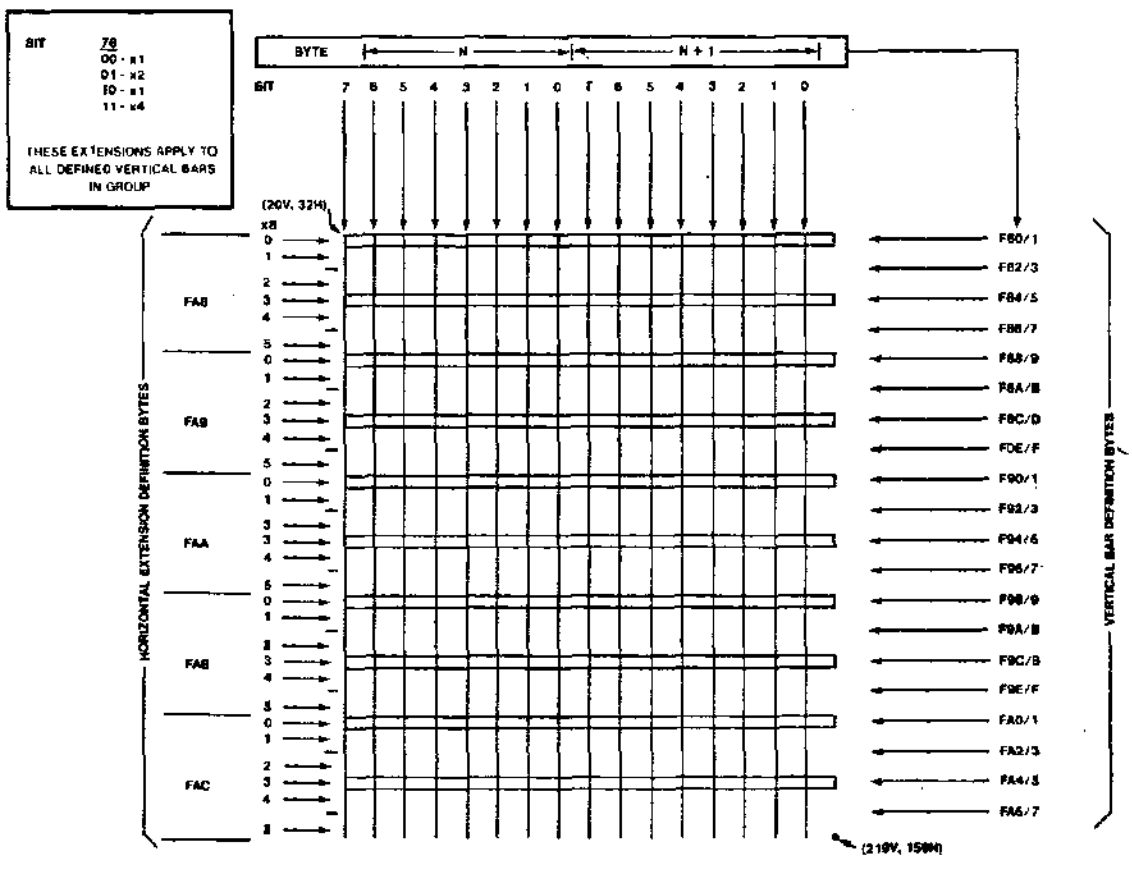


Figure 5

EXAMPLE OF BACKGROUND PROGRAMMING

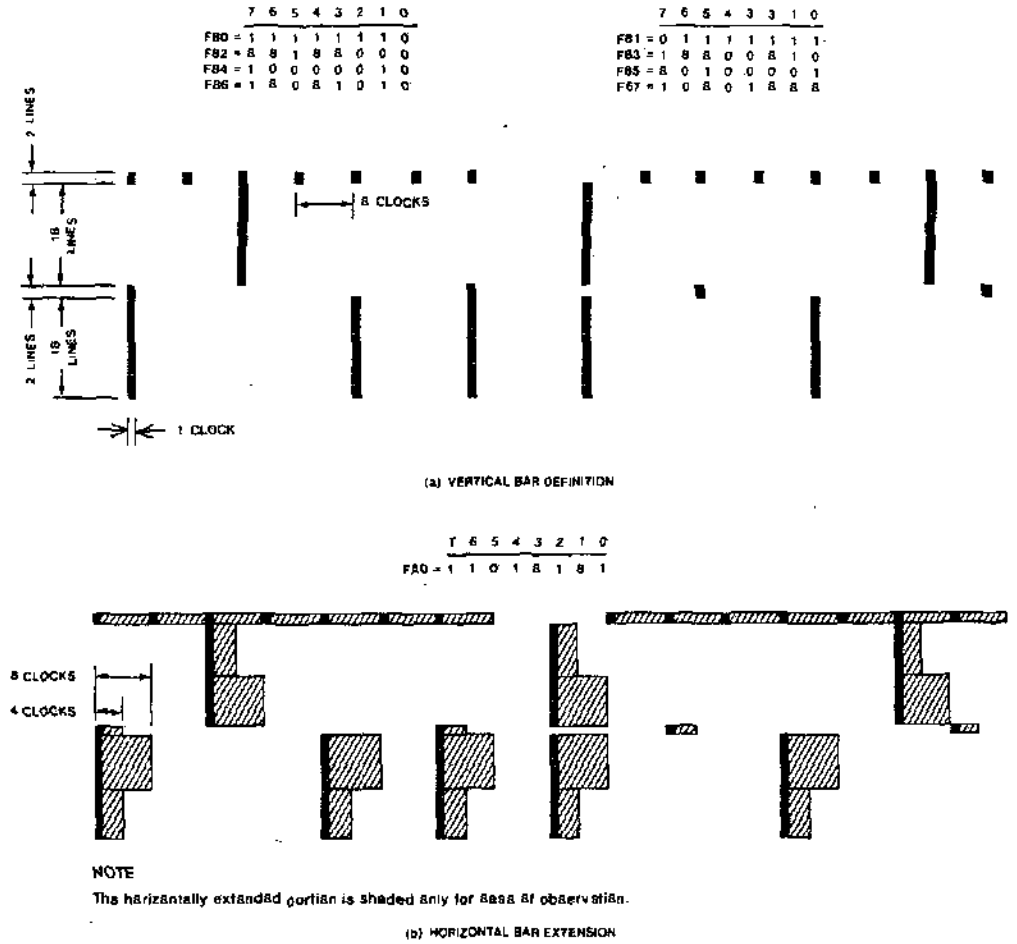


Figure 6

Bits 5-0 further divide two adjacent sets into six horizontal groups. Any bit set to 1 causes all vertical bars in that group to be eight clocks wide. For example, the bits of FA8 perform the following functions:

Bit	Function
0	Extend bars of set 1 to 8 clocks
1	Extend top 9 lines of set 2 to 8 clocks
2	Extend bottom 9 lines of set 2 to 8 clocks
3	Extend bars of set 3 to 6 clocks
4	Extend top 9 lines of set 4 to 8 clocks
5	Extend bottom 9 lines of set 4 to 6 clocks
8,7	Extend selected vertical bars of sets 1-4 to 1,2 or 4 clocks as per coding above

Figure 6b shows an example of horizontal bar extension for the previously coded vertical bars. Note that all selected bars are extended to 4 clocks because bits 7 and 6 of FA8 are '11'. In addition, certain sets are extended to 8 clocks. Figure 7 illustrates a typical complete background and its coding.

Background Enable

Background video generation is enabled by setting bit 3 of FC6 to 1 (see Figure 2).

Background Color

Background color is defined by bits 2-0 of FC6. The color behind the background (screen color) is defined by bits 6-4.

When background is not enabled, a color of '111' is output for both background and screen color. This allows "wire-OR" of background/screen color from other PVIs in multiple PVI systems.

SCORE

Four digits of score or other data may be displayed as either two separate 2-digit fields or a single 4-digit field. The four digits may be displayed at the top or at the bottom of the screen. The format and position of the score digits is controlled by the FORM and POS bits of FC3 (see Figure 2).

FORM (bit 1 of FC3) defines the data format. FORM set to 0 displays two 2-digit fields; FORM set to 1 displays one 4-digit field. POS (bit 0 of FC3) defines the data position. POS set to 0 displays the data in lines 0 to 19 of the background; POS set to 1 displays the data in lines 180 to 199 of the background. Format and positioning are illustrated in Figure 8. The N1-N4 designations correspond to N1-N4 in control bytes FC8 and FC9. The display font is shown in Figure 9. Values of A-F for N1-N4 result in a blank digit display.

EXAMPLE OF TYPICAL BACKGROUND PROGRAMMING

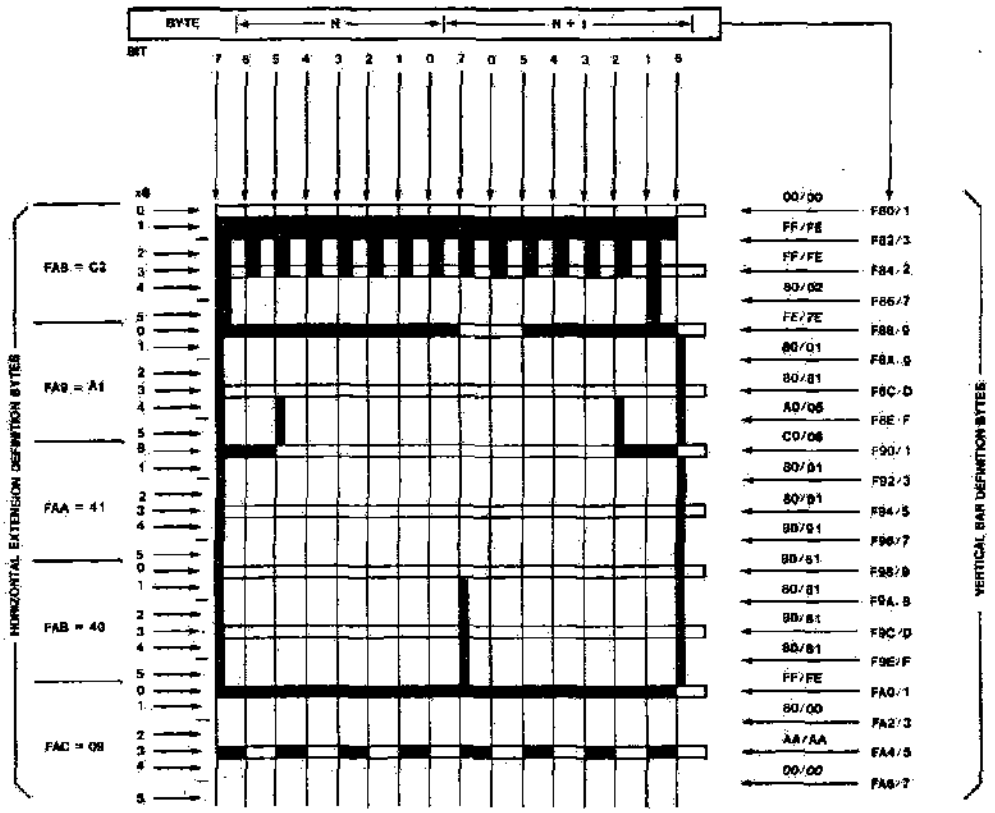


Figure 7

SCORE FORMAT AND FOSITIONING

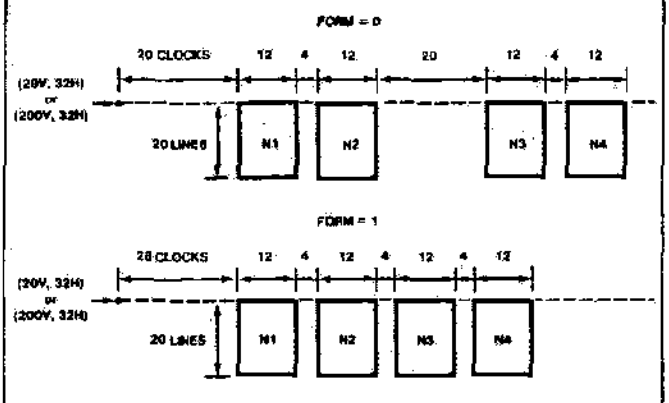


Figure 8

SCORE FONT

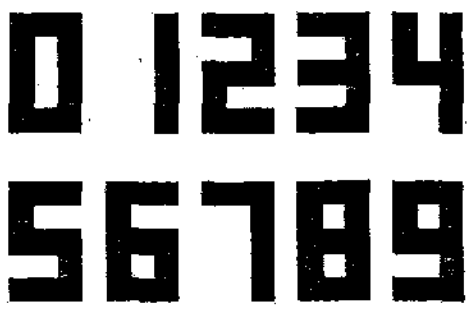


Figure 9

The color of the score digits is the same as the background color. In addition, the $\overline{OBJ/SCR}$ output is active for the score.

The top and bottom sets can be displayed simultaneously by changing the control bytes during vertical reset and between lines 40 and 199.

SOUND

The frequency of the SOUND square wave output is programmed by the value stored at FC7. A value of zero inhibits the square wave output. Other values result in a square wave period equal to $2(n+1)T_H$ where n is the value of SOUND and T_H is the horizontal reset period (normally 63.5µs).

If SOUND is changed while a frequency is being generated (SOUND ≠ 0), the new value will not become effective until the next positive or negative transition of the SOUND output.

ANALOG TO DIGITAL CONVERTERS

Two internal A/D converters are provided for conversion of potentiometer data to digital values. Conversion takes place during the active vertical scan and the data, which is stored at FCC and FCD, is valid only during vertical reset. When using the recommended input R-C combination (see SPECIFICATIONS section), values ranging from a maximum low value of 20 to a minimum high value of 225 are obtained.

COLOR SYSTEM

Six 3-bit variables are assigned to locations within the PVI memory, one for each of the four objects, one for background, and one for screen color (i.e., background video = 0).

The possible simultaneous presentation of video (object/background/score) requires color precedence resolution as follows: colors of objects are wire-OR'ed and take precedence over background, screen and score color.

An additional pin representing the logical 'OR' of all score and object video is available. This may be used as a luminance control signal to differentiate between background and objects.

VERTICAL RESET STATUS BIT

VRLE (bit 6 of FCB) is set at the leading edge of the vertical reset signal. It is automatically cleared when FCB is read or at the trailing edge of vertical reset.

ABSOLUTE MAXIMUM RATINGS [1,3]

PARAMETER	RATING	UNIT
Supply voltage	6.0	V
Storage temperature	−65 to +150	°C
Operating temperature[2]	0 to +55	°C
Minimum voltage, any pin	−0.3	V
Maximum voltage, any pin	6.0	V

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent changes to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of the specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designated for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[4,5,6,7] T_A = 0°C to +55°C, V_{CC} = 5V ±5%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH}	Input low level Input high level	All inputs except POT1, POT2	0 2.2		0.8 V_{CC}	V V
V_{OL}	Output low level C1, C2, C3, OBJ/SCR outputs OPACK, INTREQ outputs D0-D7, CE1, CE2, sound outputs	 I_{OL} = 2.8mA I_{OL} = 2.0mA I_{OL} = 1.6mA	 0 0 0		 0.45 0.45 0.45	 V V V
V_{OH}	Output high level D0-D7, CE1, CE2, Sound other outputs	I_{OH} = −100µA 5kΩ to V_{CC}	2.4 2.4		V_{CC} V_{CC}	V V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}V			10	µA
I_{OLH}	Data bus Tri-State leakage	V_{OUT} = 4.0V			10	µA
I_{OLL}	Data bus Tri-State leakage	V_{OUT} = 0.45V			−10	µA
I_{CC}	Supply current			120	160	mA
C_{IN}	Input capacitance	V_{IN} = 0V			20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V			20	pF
R_{MIN}	POT1, POT2 INPUTS Minimum resistance to V_{CC} Maximum A/D value[11,12] Minimum A/D value[11,12]	 R = 15K to V_{CC}, C = 0.1µF R = 515K to V_{CC}, C = 0.1µF	15 225		 20	KΩ

NOTES

4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IL}, V_{IL} levels as appropriate.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. In normal operation, the PCK, HRST and VRST inputs for the 2636 and the CLOCK input for the 2650A are obtained from the 2622 Universal Sync Generator. See 2622 data sheet for timing of these signals.
8. This parameter is specified only to establish the timing reference pulses P1-P5.
9. Applies when PVI internal address field (F00-FFF) is addressed and PVI is not performing an internal operation. If PVI is performing an internal operation, occurrence of P2 will be delayed an integral number of PCK clock cycles.
10. Applies when either of the chip enable output address fields is addressed.
11. Count Valid when VRST = High.
12. For 312 line PAL format special precautions must be taken to prevent POT1, POT2 count wrap-around.

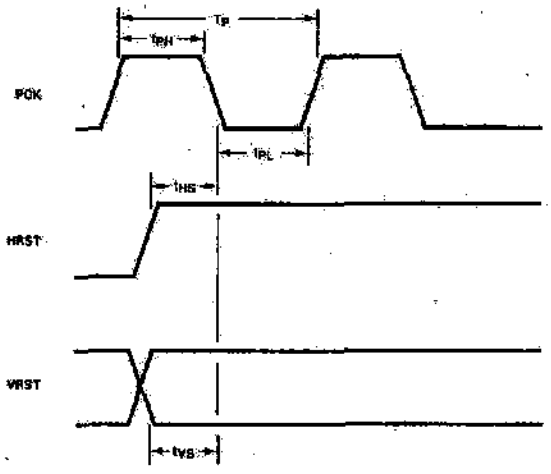
AC ELECTRICAL CHARACTERISTICS[4,5,6,7] T_A = 0 to +55°C, V_{CC} = 5V ±5%

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
T_p	PCK clock period		280			nS
t_{PL}	PCK pulse width, low		90	100		nS
t_{PH}	PCK pulse width, high		90	100		nS
t_{HS}	HRST setup		0		t_{PH}	nS
t_{VS}	VRST setup		0		t_{PH}	nS
t_{OS}	OPREQ setup[8]		50			nS
t_{AS}	Address setup		50			nS
t_{AH}	Address hold		50			nS
t_{RWS}	R/W setup		50			nS
t_{RWH}	R/W hold		50			nS
t_{AKL1}	$\overline{OPACK}$ low delay[9]	C_L = 100pF, R_L = 5kΩ to V_{CC} OR			175	nS
t_{AKH1}	$\overline{OPACK}$ high delay[9]			1000		nS
t_{AKL2}	$\overline{OPACK}$ low delay[10]	C_L = 50pF, R_L = 10kΩ			250	nS
t_{AKH2}	$\overline{OPACK}$ high delay[10]	to V_{CC} and 1 TTL load		1000		nS
t_{DD}	Data delay time for READ	C_L = 50pF 1 TTL Load			450	nS
t_{DV}	Data valid time for READ		2.0			µS
t_{DF}	Data bus floating time for READ				300	nS
t_{DS}	Data bus setup for WRITE		0			nS
t_{DH}	Data bus hold for WRITE		100			nS
t_{CEON}	Chip enable on delay	C_L = 50pF 1 TTL Load			400	nS
t_{CEOF}	Chip enable off delay				300	nS
t_{VL}	Video leading edge delay	C_L = 30pF R_L = 1.8kΩ to V_{CC}			200	nS
t_{VT}	Video trailing edge delay				200	nS
t_{VR}	Video rise time			100		nS
t_{VF}	Video fall time			100		nS

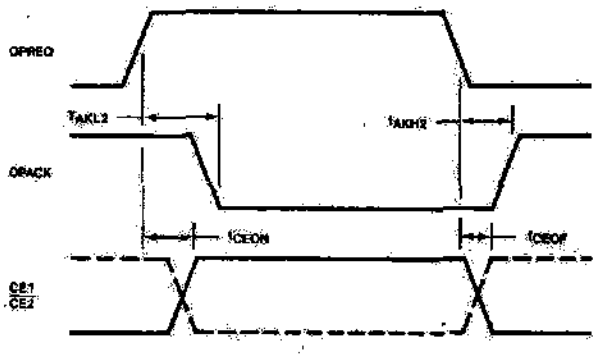
NOTES
See previous page

TIMING DIAGRAMS

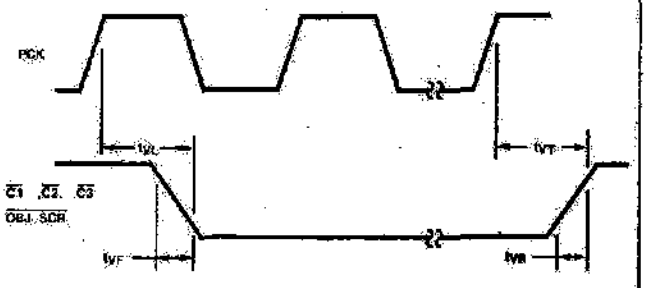
CLOCK SIGNAL TIMING



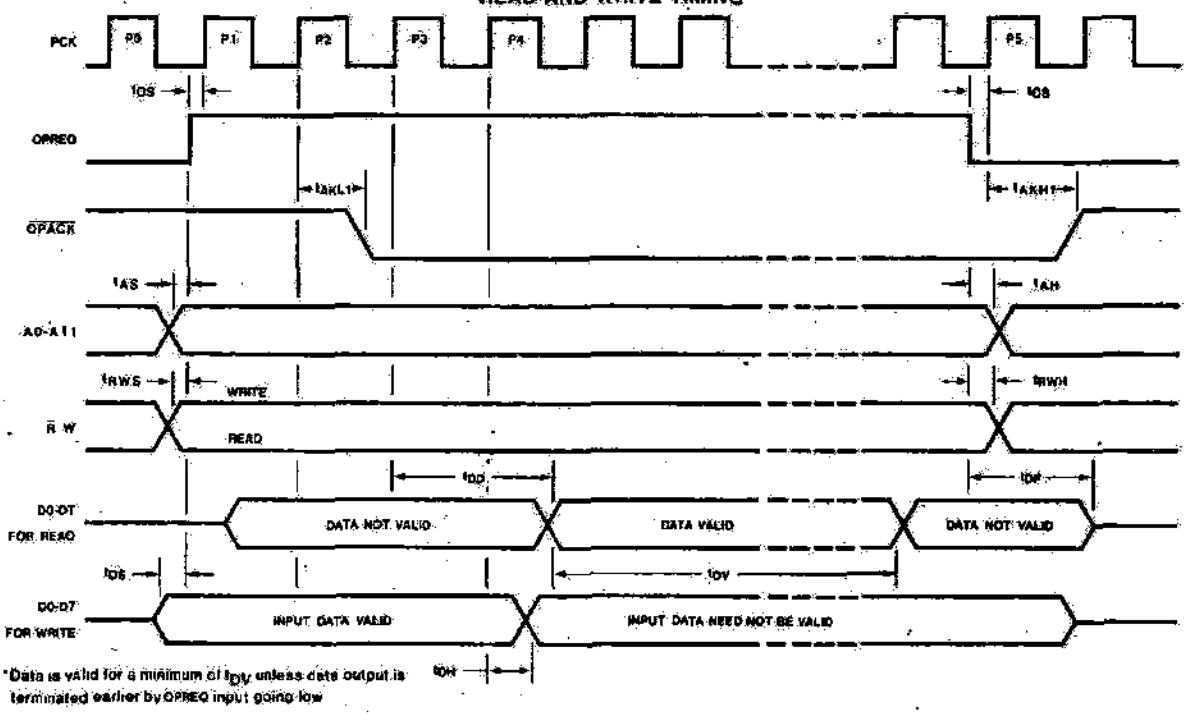
OPACK AND CHIP ENABLE TIMING



VIDEO OUTPUT TIMING



READ AND WRITE TIMING



*Data is valid for a minimum of t_{DV} unless data output is terminated earlier by OPREQ input going low