F2114/2114L
1024 x 4 Static RAM

MOS Memory Products

Description

The F2114 is a 4096-bit static Random Access Memory (RAM) organized as 1024 words of four bits each. Since the operation of the F2114 is entirely static, there is no clocking or refreshing required. It operates from a single +5 V supply and is directly a TTL compatible at all inputs and outputs including the four bidirectional data I/O pins.

It is designed for memory applications in which static operation, large bit-capacity, and simple interfacing are important design considerations.

The F2114 is manufactured using Fairchild's n-channel silicon gate Isoplanar process. The innovative use of polysilicon resistors in the static memory cell permits a high bit packing density and insures low-power characteristics. It is available in a standard plastic or ceramic 18-pin dual in-line package.

- **1024 x 4-BIT ORGANIZATION**
- **SINGLE +5 V SUPPLY**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **TOTALLY TTL COMPATIBLE**
- **COMMON DATA I/O PINS WITH 3-STATE CAPABILITY**
- **IDENTICAL CYCLE AND ACCESS TIMES**
- **LOW POWER (2114L)**

Pin Names

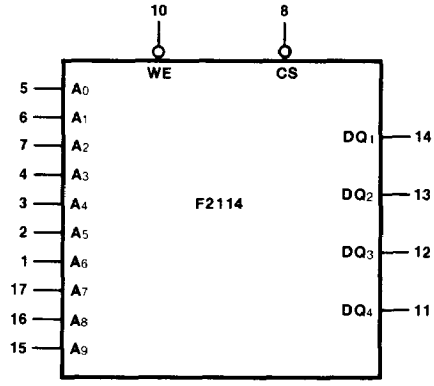
A_0-A_9	Address Inputs
$\overline{CS}$	Chip Select (Active LOW)
$\overline{WE}$	Write Enable (Active LOW)
DQ_1-DQ_4	Data Input/Output
V_{CC}	+5 V Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage at Any Pin with Respect to GND	−0.5 V to +7.0 V
Operating Temperature (Ambient)	0°C to +70°C
Storage Temperature (Ambient)	−55°C to +150°C
Power Dissipation	1 W

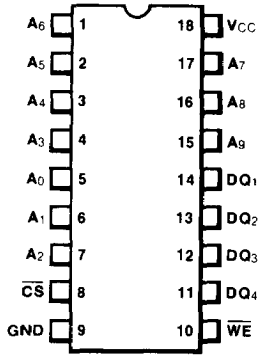
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

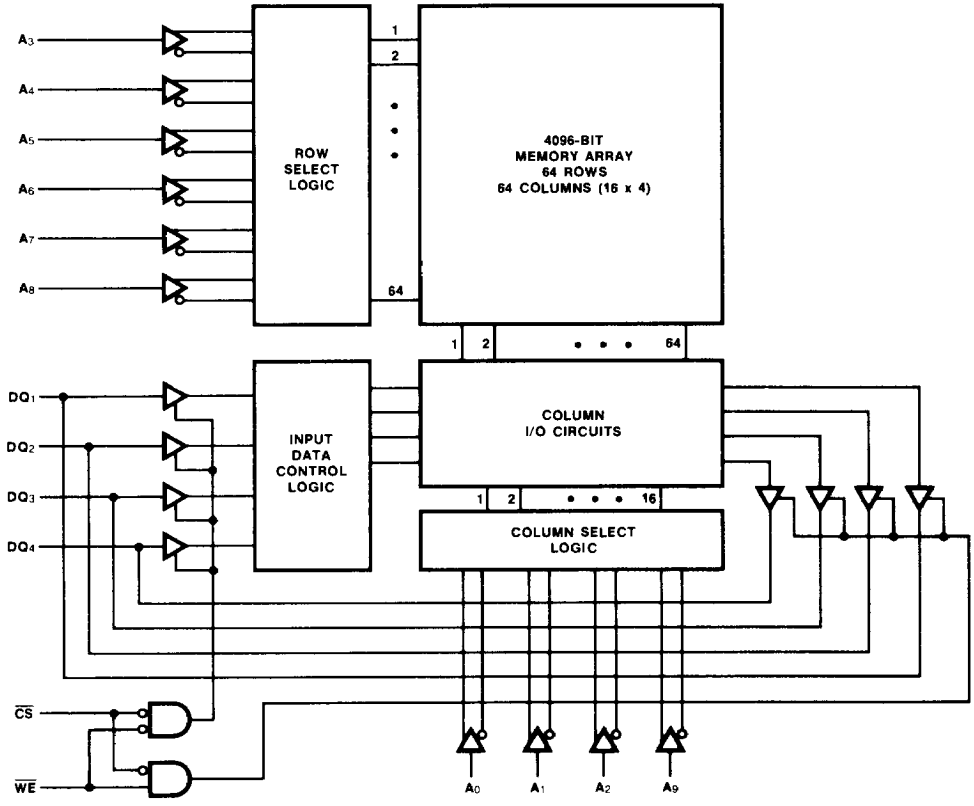
Connection Diagram
18-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	8D	D
Plastic DIP	8J	P

Block Diagram



Functional Description

The F2114, organized as 1024 words by four bits, is controlled by the Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) and the ten address inputs. When $\overline{CS}$ goes HIGH the memory becomes deselected; the bidirectional input/output pins become high impedance, and the $\overline{WE}$ input is ignored. Therefore no read or write operations may occur. This feature allows the DQ pins to be OR-tied directly to a data bus. When the memory is selected ($\overline{CS}$ LOW), and the $\overline{WE}$ pin is in the HIGH state, the 4-bit word stored at the memory location specified by the address inputs is gated through to the DQ pins after a delay equal to the access time. If the $\overline{WE}$ is forced LOW, then the DQ pins become HIGH impedance inputs so that an externally supplied data word may be placed on them.

All inputs and bidirectional DQ pins are directly TTL compatible with data always being read out in the same polarity as it was written (i.e., not inverted).

Truth Table

$\overline{CS}$	$\overline{WE}$	DQ	Comments
H	X	High Z	Chip Deselected
L	L	H	Write "1"
L	L	L	Write "0"
L	H	Data	Read

DC Electrical Requirements and Characteristics T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%, all voltages are with respect to ground, Note 1

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OUT} = −1.2 mA
V_{OL}	Output LOW Voltage	0		0.4	V	I_{OUT} = 3.2 mA
I_{OS}	Output Short-Circuit Current, Note 2			65	mA	V_{OUT} = 0 V
I_{CC}	Average V_{CC} Supply Current F2114L2, F2114L3, F2114L			70	mA	V_{CC} = 5.25 V, T_A = 0°C,
	Average V_{CC} Supply Current F2114-2, F2114-3, F2114			100	mA	V_{IN} = 5.25 V, I/O current = 0 mA
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.25 V
I_{DQ}	I/O Leakage Current	−10		10	μA	$\overline{CS}$ = 2.0 V, $V_{I/O}$ = 0.4 V to V_{CC}
C_{IN}	Input Capacitance			5.0	pF	T_A = 25°C, f = 1.0 MHz V_{IN} = 0 V
C_{DQ}	I/O Capacitance			5.0	pF	T_A = 25°C, f = 1.0 MHz $V_{I/O}$ = 0 V

AC Electrical Requirements And Characteristics T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 5%, Notes 1 and 3

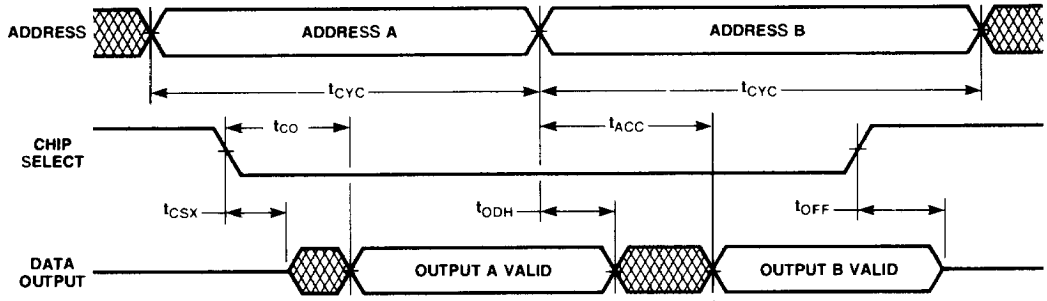
		F2114L-2 F2114-2		F2114L-3 F2114-3		F2114L F2114			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Note
t_{CYC}	Read or Write Cycle Time	200		300		450		ns	
t_{ACC}	Read Access Time		200		300		450	ns	
t_{CO}	$\overline{CS}$ LOW to Output Valid Delay		70		100		100	ns	
t_{CSX}	$\overline{CS}$ LOW to Output Active Delay	20		20		20		ns	
t_{ODH}	Output Data Hold Time After Address	50		50		50		ns	
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CS}$	0	60	0	80	0	100	ns	
t_{AW}	Address to Write Set-up Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	120		150		200		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DS}	Input Data Set-up Time	120		150		200		ns	
t_{DH}	Input Data Hold Time	0		0		0		ns	

Notes

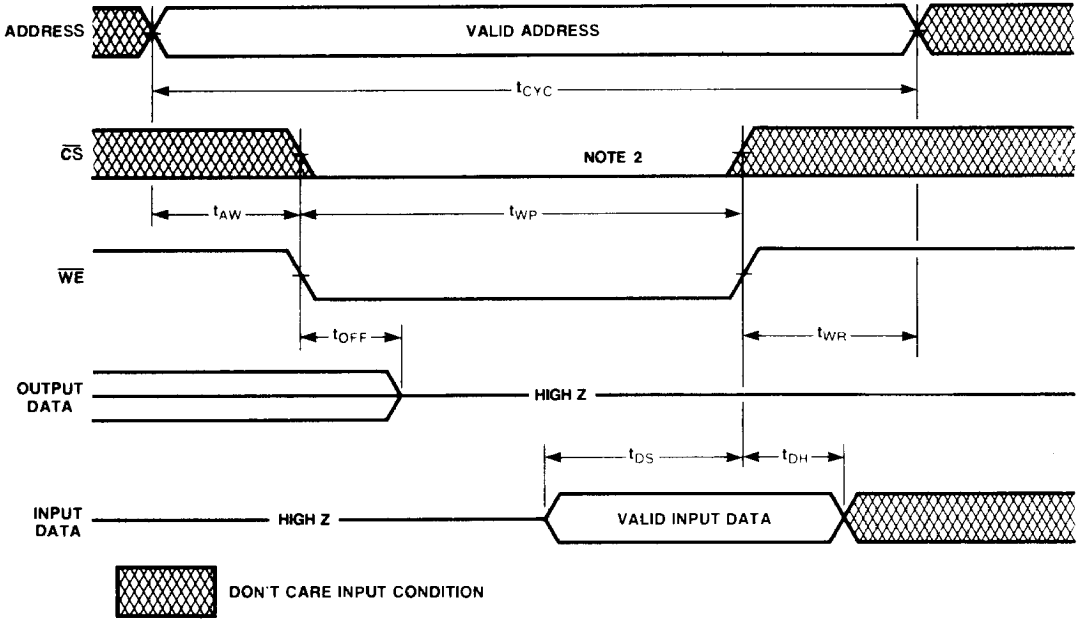
1. Test Note: The F2114 employs a self starting oscillator and a charge pump which require a start-up time of 500 μs after V_{CC} reaches at least 4.75 V.
2. Duration not to exceed 30 seconds.
3. AC Characteristic Test Conditions:

Input Levels	0.8 to 2.0 V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5 V
Output Load	1 TTL Gate, and CL = 100 pF

Read Mode Timing Diagram, Note 1



Write Mode Timing Diagram



Notes

1. $\overline{WE}$ must remain HIGH during READ cycles.
2. t_{WP} is measured from the falling edge of either $\overline{CS}$ or $\overline{WE}$ (whichever is the last to go LOW) to the rising edge of either $\overline{CS}$ or $\overline{WE}$ (whichever is the first to go HIGH).