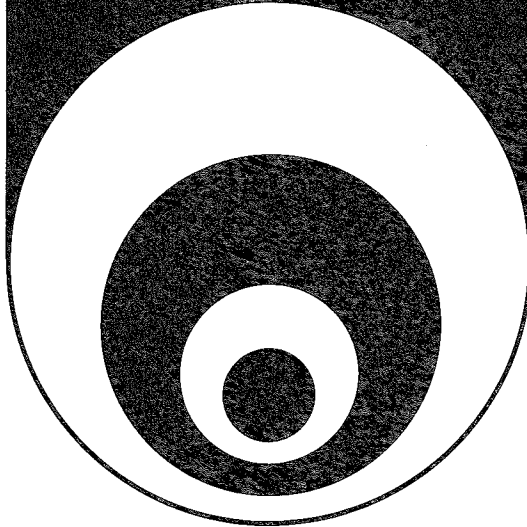


**signetics**

**MICROPROCESSOR**



SERIAL INPUT/OUTPUT.....AS50

## 2650 MICROPROCESSOR APPLICATION MEMO

### INTRODUCTION

The Sense/Flag capability of the Signetics 2650 microprocessor can be used for serial I/O interfaces. The Sense input pin is directly connected to a bit in the microprocessor's Program Status Word. A high level on the Sense pin appears as a binary one while a low level appears as a binary zero. The Sense bit in the PSW can be stored or tested by the program. The Flag bit in the PSW is a simple latch that drives the Flag output pin. A program can set the Flag bit to a binary one, which causes a high level, one TTL load on the flag output pin. Setting the Flag bit to binary zero causes a low level on the Flag output pin.

### APPLICATIONS

The most common use for the Sense/Flag capability would be in interfacing to a keyboard based terminal where the data is received or transmitted as bit serial. All bit manipulation and timings such as 8-bit serial-to-parallel conversion can be done by software running on the 2650. The software works by storing or setting the two bits in the Program Status Word which reflect or control the levels at the pins of the chip. External hardware is required simply to interface with line levels. No clock synchronization or address decoding hardware is necessary, since the Sense and Flag pins are independent of the normal I/O bus structure.

Two examples of device interfaces and software are given below; for a 1200 baud RS232-type CRT terminal and for a 110 baud Teletype. Figure 1 shows the RS232 interface. Half of the Signetics 8T15 dual line driver is used to transmit to the terminal from the Flag pin, while half of a

Signetics 8T16 dual line receiver is used to receive from the device into the Sense pin. The interface to a Teletype model 33 is shown in Figure II. A TTL open collector gate is used to provide the 20 milli-amp loop to the TTY

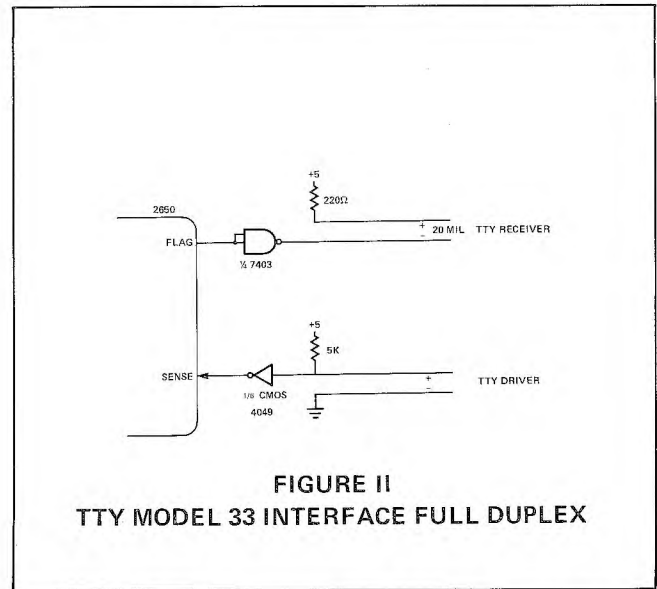


FIGURE II  
TTY MODEL 33 INTERFACE FULL DUPLEX

receiver. For receiving from the TTY a CMOS gate is used to provide the necessary noise immunity.

### SOFTWARE

All definitions of baud rate, character formats, and line characteristics are done in the software. For these examples, communication is asynchronous bit-serial over a full duplex line. Figure III shows the format of a 8-bit character (seven bits plus parity) headed by a start bit and followed by stop bits. The line levels are:

- low = start bit or binary zero
- high = stop bit or binary one

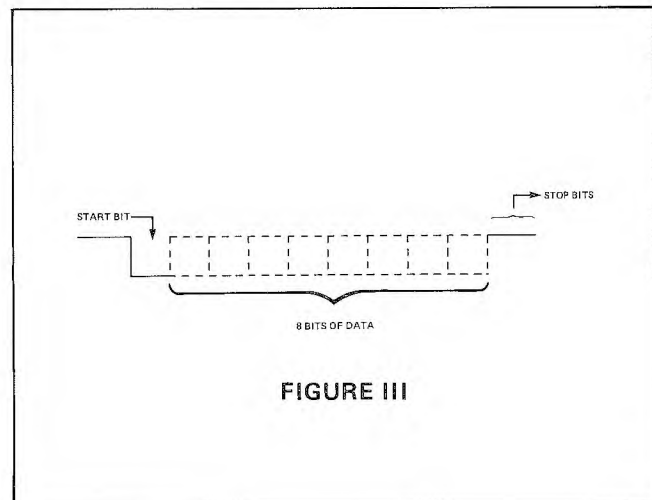


FIGURE III

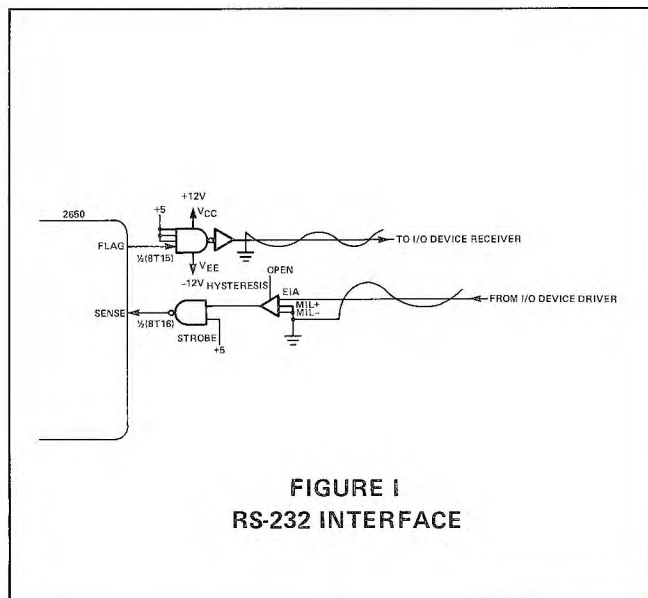


FIGURE I  
RS-232 INTERFACE

```

PIP ASSEMBLER VERSION 2 LEVEL 1
PAGE 1
LINE ADDR LABEL B1 B2 B3 B4 ERROR SOURCE
1 0001 *
2 0002 P EQU 0
3 0003 N EQU 1
4 0004 LCOM EQU H'02* LOGICAL COMPARE
5 0005 CAM EQU H'01* CARRY
6 0006 SENS EQU H'80* SENSE
7 0007 FLAG EQU H'40* FLAG
8 0008 I EQU H'20* INTERRUPT INHIBIT
9 0009 IDC EQU H'04* INTER DIGIT CARRY
10 0010 OVF EQU H'06* OVEFLOW
11 0011 R0 EQU 0
12 0012 R1 EQU 1
13 0013 R2 EQU 2
14 0014 R3 EQU 3
15 0015 UN EQU 0
16 0016 ED EQU 0
17 0017 LT EQU 0
18 0018 GT EQU 0
19 0019 WC EQU H'08*
20 0020 HS EQU H'500*
21 0021 *
22 0022 *
23 0500 0500 76 40 CHIO PPSU WC FLAG INPUT WITH A BIT BY BIT ECHO
24 0502 0502 0E 00 CPSL
25 0504 0504 0E 00 LDDI,R1
26 0506 0506 0E 08 LDDI,R2
27 0508 0508 1A 7D TEST RCTR,LT TEST LOOP TESTS FOR THE START BIT
28 0509 0509 3F 05 29 DLY BSTA,UN DLY HALF A DELAY TO MIDDLE OF BIT
29 050E 050E 74 40 BIT CPSU FLAG DELAY, THEN READ THE NEXT BIT
30 0510 0510 3F 05 2D BIT BSTA,UN DLY
31 0512 0512 12 44 80 SPSU
32 0514 0514 51 61 ANDI,R0 H'80*
33 0516 0516 51 61 RRR,R1
34 0517 0517 61 61 TONZ R1
35 0518 0518 61 61 STZ R1
36 0519 0519 1A 04 RCTR,LT ZERO ECHO THE BIT
37 051E 051E 74 40 PPSU FLAG
38 051D 051D 1B 02 SCTR,UN NEXT
39 051F 051F 76 40 ZERU PPSU FLAG
40 0521 0521 74 40 NEXT BRR,R2 H'1*
41 0521 0521 3F 05 2D NEXT BSTA,UN DLY
42 0526 0526 45 7F ANDI,R1 H'7F*
43 0528 0528 17 RETC,UN
44 *
45 *
46 *
47 0529 0529 04 3A DLY LDDI,R0 H'5A*
48 052B 052B 1B 02 DLY BCTR,UN DLY
49 052D 052D 04 59 DLAY LDDI,R0 H'59*
50 052F 052F 78 7E DL1 BRR,R0 $
51 0531 0531 17 RETC,UN $
52 *
* TIMING DELAY FOR 1200 BAUD RS232 TERMINAL
* TIMING DELAY FOR 110 BAUD TELETYPE

```

```

PIP ASSEMBLER VERSION 2 LEVEL 1
PAGE 2
LINE ADDR LABEL B1 B2 B3 B4 ERROR SOURCE
53 0532 0532 20 TDLA EDNZ R0
54 0533 0533 78 7E BRR,R0 $
55 0535 0535 78 7E BRR,R0 $
56 0537 0537 78 7E BRR,R0 $
57 0539 0539 04 55 LDDI,R0 H'E5*
58 053B 053B 78 7E BRR,R0 $
59 053D 053D 17 RETC,UN
60 END
TOTAL ASSEMBLER ERRORS = 0

```

FIGURE IV

The internal logic of the program shown in Figure IV (the program listing) is to sense each incoming bit of the character and to output the bit in turn for the full duplex line. The Sense input is tested in the loop at 'TEST' for the transition to zero indicating the start bit. The program then delays one half of a bit time to the center of the start bit. At this point the echoing of the character starts by clearing the Flag bit which outputs the start bit transition. At 'BIT' the program then delays one full bit time to the center of the data bit. The Sense line is tested and that bit value is rotated into register one. The bit value is then used to set or clear the Flag bit for the echo. At 'NEXT' is the test

that controls the loop to get only eight bits. Figure V is a picture of the levels and timings when echoing a 'U'.

The bit timing is done by a subroutine which simply counts cycles for the appropriate baud rate. The example program shows both a 1200 baud delay at 'DLAY' and a 110 baud delay at 'TLAY'. The conversion from instruction cycles to milliseconds is based on a 1MHz clock rate. Clock stability is only moderately important since each character involves only nine sample times and each start bit redefines the base line for all timings.

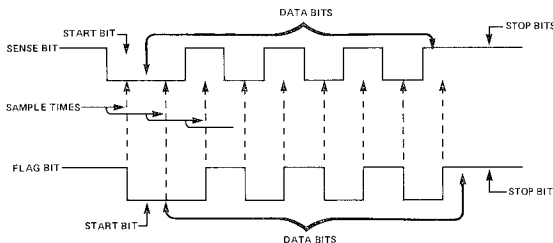


FIGURE V



811 EAST ARGUES AVENUE ■ SUNNYVALE, CALIFORNIA ■ 94086 ■ TEL: (408) 739-7700