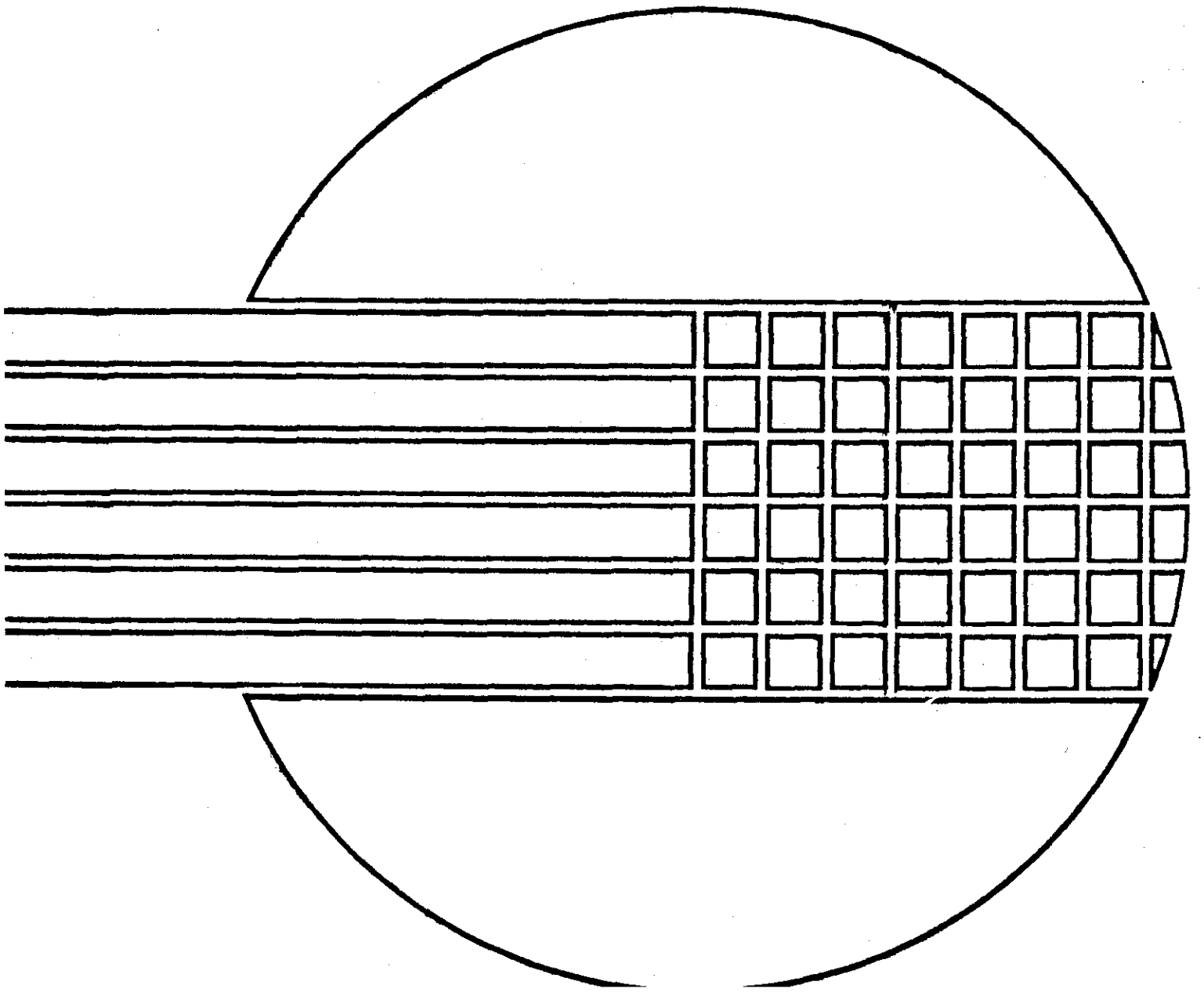
SIGNETICS UNIVERSAL SYNC GENERATOR (PAL) 2621



PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics 2621 Universal Sync Generator (USG) provides the timing and control signals necessary for generating and displaying TV video information in the PAL format.

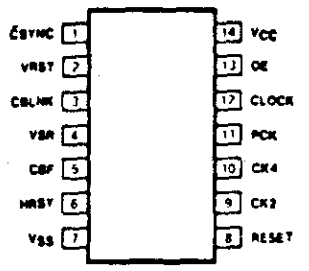
The USG accepts a single 3.55MHz input clock and generates various timing outputs including vertical, horizontal and composite blanking, composite sync and color burst flag. Several auxiliary clock outputs are also provided.

The USG is primarily intended for use in microprocessor-controlled video games. A typical game configuration consists of a 2621 USG, a 2650A microprocessor, a 2636 Programmable Video Interface, a 2616 16K ROM, and digital video summer circuitry.

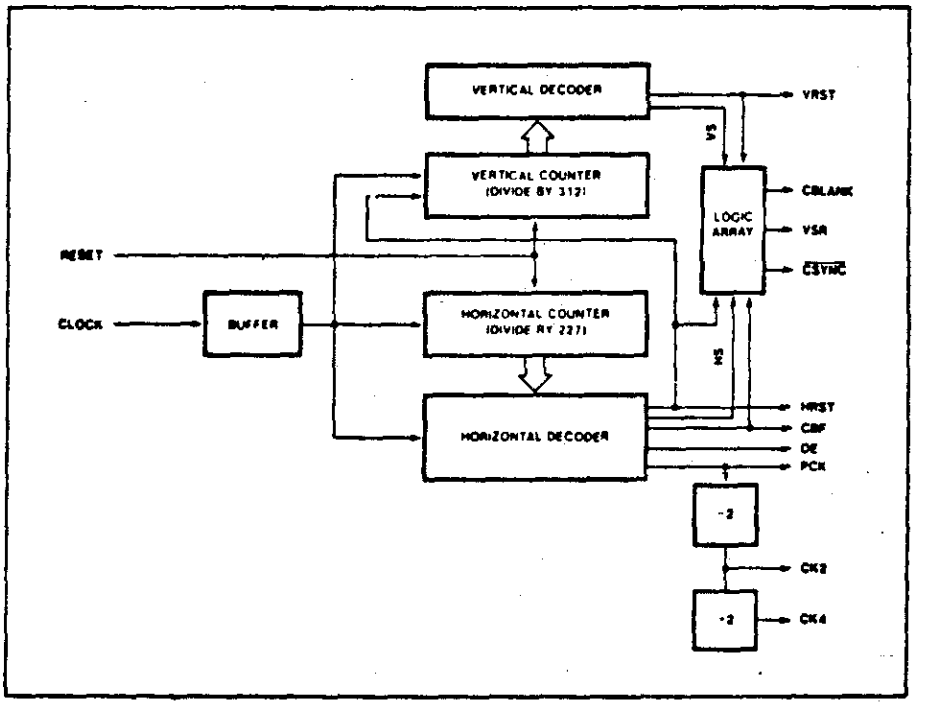
The 2621 is constructed using Signetics silicon gate N-channel depletion load technology and operates from a single +5 volt power supply.

PIN CONFIGURATION

NH PACKAGE



BLOCK DIAGRAM



PRELIMINARY SPECIFICATION

PIN OESIGNATION

PIN NO.	MNEMONIC	TYPE	NAME & FUNCTION
1	$\overline{CSYNC}$	Output	**Composite Sync:** PAL non-interlaced composite sync output.
2	VRST	Output	**Vertical Reset:** Vertical reset output.
3	CBLNK	Output	**Composite Blanking:** Modified PAL non-interlaced composite blanking output.
4	VSR	Output	Test output.
5	CBF	Output	**Color Burst Flag:** PAL non-interlaced color burst flag output.
6	HRST	Output	**Horizontal Reset:** Horizontal reset output.
7	V_{SS}	Input	Ground.
8	RESET	Input	**Reset:** A high input resets the horizontal and vertical counters. Used for test only
9	CK2	Output	**Clock 2:** A clock output which is PCK divided by two.
10	CK4	Output	**Clock 4:** A clock output which is PCK divided by four.
11	PCK	Output	**Position Clock:** Horizontal position clock output. Contains 227 cycles of 282n in each horizontal period.
12	CLOCK	Input	**Clock:** Clock input. Normally 3.55MHz.
13	OE	Output	**Odd/Even:** Odd/Even line output.
14	V_{CC}	Input	**Power Supply:** +5V ±5%

ABSOLUTE MAXIMUM RATINGS [1,3]

PARAMETER	RATING	UNIT
Supply voltage	6.0	V
Storage temperature	−65 to +150	°C
Operating temperature[2]	0 to +55	°C
Minimum voltage, any pin	−0.3	V
Maximum voltage, any pin	6.0	V

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 150°C/W junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the V_{OH}, V_{OL}, V_{IH}, V_{IL} levels as appropriate.
6. Typical values are at +25C, typical supply voltages and typical processing parameters.
7. Applies to CBLNK, $\overline{CSYNC}$, CBF, HBLNK, VSLNK.

PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

PRELIMINARY SPECIFICATION

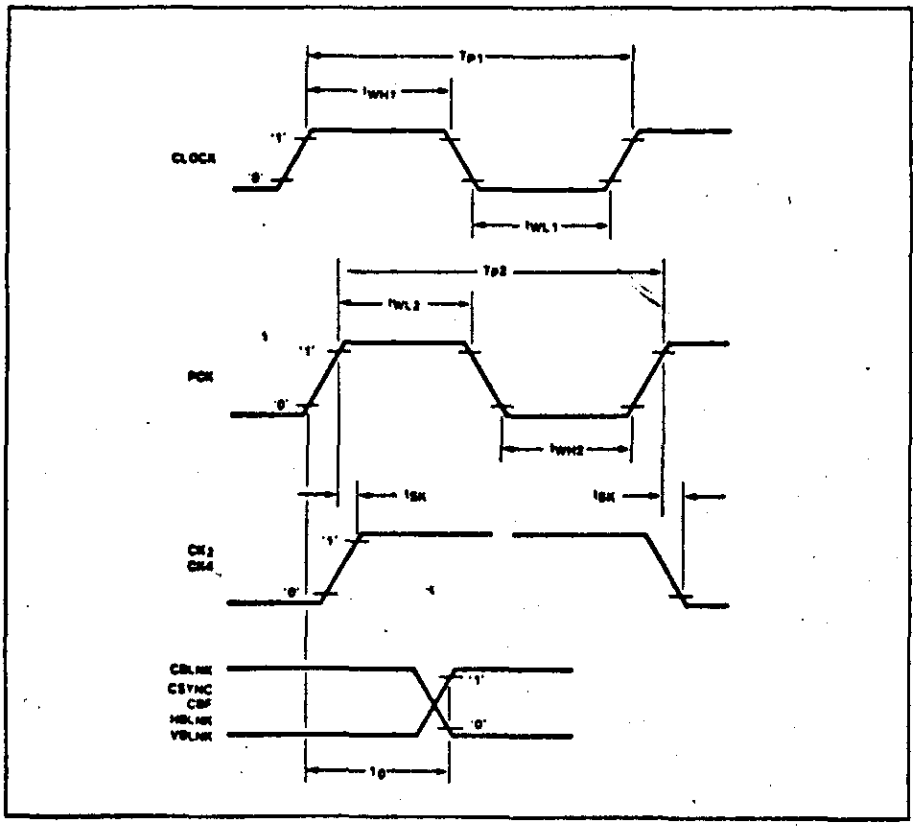
DC ELECTRICAL CHARACTERISTICS [4,5,6] T_A = 0°C to +55°C, V_{CC} = 5V ±5%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low level		0		0.8	V
V_{IH}	Input high level		2.2		V_{CC}	V
V_{OL}	Output low level	I_O = +400μA	0		0.45	V
V_{OH}	Output high level	I_O = −100μA	2.4		V_{CC}	V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.25V			10	μA
I_{CC}	Supply current	V_{CC} = 5.25V			60	mA
C_{IN}	Input capacitance	V_{IN} = 0V, f = 1MHz			20	pF
C_{OUT}	Output capacitance	All other pins grounded			20	pF

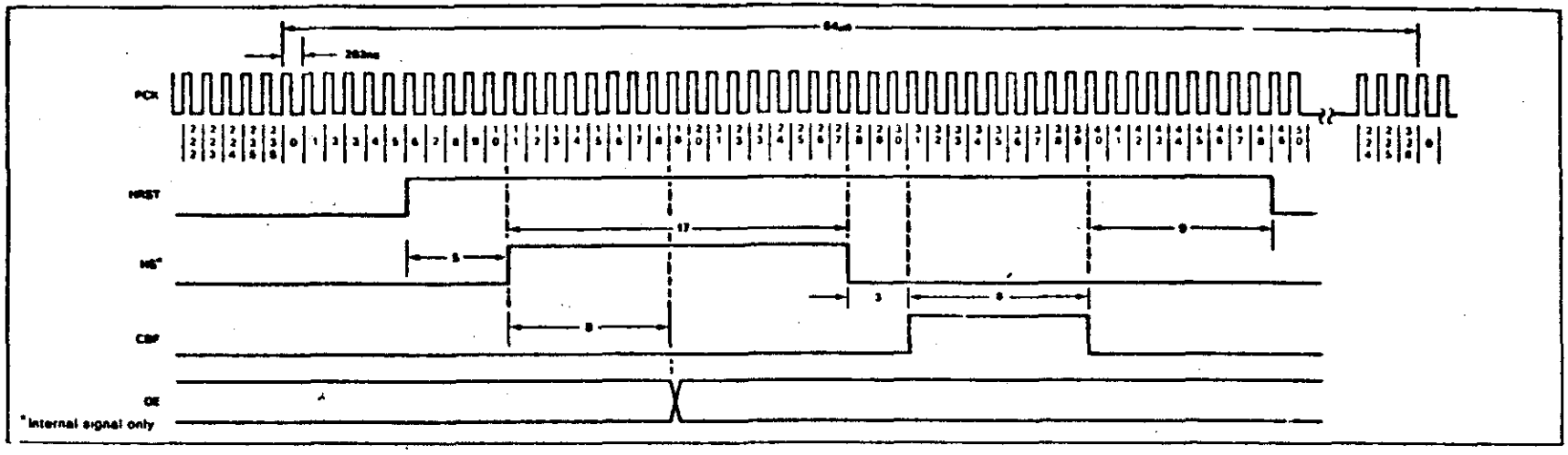
AC ELECTRICAL CHARACTERISTICS, [4,5,6] T_A = 0°C to +55°C, V_{CC} = 5V ±5%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{WL1}	Clock pulse width low		100			ns
t_{WH1}	Clock pulse width high		100			ns
T_{p1}	Clock period			282		ns
t_{WL2}	PCK pulse width low	C_L = 50pF		100		ns
t_{WH2}	PCK pulse width high	C_L = 50pF		100		ns
T_{p2}	PCK period	C_L = 50pF		282		ns
t_{SK}	CK2, CK4 skew from PCK	C_L = 50pF			50	ns
t_D	Output signal delay[7]	C_L = 75pF			100	ns

TIMING DIAGRAMS



HORIZONTAL TIMING



VERTICAL TIMING